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Interface Controlled Organic Thin Films

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Interface Modification of Pentacene OFET Gate Dielectrics

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Abstract. Pentacene organic field effect transistors (OFETs) electrical and structural properties have already been analysed from the point of view of different gate dielectric and growth conditions utilization. The AFM and micro Raman investigations show that the first organic monolayer at the pentacene/dielectric interface are essential determinants of carrier transport phenomena and achievable drain current of pentacene OFETs.

1. Introduction

Pentacene is one of the leading candidates of the many organic materials available, for use in current organic field-effect transistor (OFET) architectures, because of its excellent electrical characteristics and its resistance to atmospheric oxygen [1]. Manipulating the semiconductor/dielectric interfacial properties via optimising the gate dielectric can substantially enhance OFET performance [2,3]. Parylene's superior electrical insulation characteristics make it an excellent solution for the OFETs gate dielectric. In this work we present pentacene/gate dielectric interface modification with thin parylene layers and self-assembled monolayer (SAM) of diacetylene formed by the Langmuir-Blodgett method.

2. Experimental Methods

In order to understand the pentacene thin films growth on different dielectric materials we studied the growth of pentacene molecules on three different substrate materials SiO_2, SiO_2 covered with diacetylene SAM formed by the Langmuir-Blodgett method and SiO_2 covered with thin parylene layer. Pentacene bottom gate top contact OFET structures were prepared on silicon substrate (gate) covered with thermal grown 40 nm thick silicon dioxide with these different dielectric layers to compare their electrical properties. The polymer parylene C has been chosen as a gate insulator material, which forms transparent pinhole–free conformal coatings with excellent dielectric. High purity dichloro-di-para-xylylene was used for chemical

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vapour deposition process to create high quality thin parylene C layers 20 and 40nm thick. The pentacene films were prepared from commercially available material (Acros Organic) with 98% purity. Pentacene was deposited by thermal evaporation at substrate temperature of 30, 50 and 70°C and deposition rate 0,2 – 0,5 Å/s. For preparation of the OFET with the top electrodes structure, gold source and drain electrodes with different channel length (15, 25, 45 μm) and 2000 μm channel width were deposited thermally thru the shadow mask on 40 nm pentacene layer.

3. Results and Discussion

Figure 1 show output characteristics of the organic pentacene OFETs prepared on different SiO_2, SAM and parylene dielectric layers at constant gate voltage $V_G = -20$ V. A significant increase of the source–drain current were measured for OFETs prepared on parylene layers in comparing with devices prepared on SiO_2 based interface layers. The highest value of the drain current was reached for pentacene layer prepared at 30°C on parylene dielectric layer. The measured output characteristics in dependence on gate voltage are shown in Fig. 2, corresponding to charge mobility of 0.15 $cm^2V^{-1}s^{-1}$. The analysis of the measured results shows the pentacene/dielectric interface has considerably influence on the carrier transport phenomena. This was confirmed by AFM investigations of the thin pentacene layers prepared at different growth temperature 30 and 70°C on parylene layers. As shown in Fig. 3, 4 the pentacene layer growing at 30°C shows better crystalline structure formation. For the thick 40 nm pentacene layer prepared at 30°C on parylene dielectric the AFM image (Fig. 5) shows creation of two crystalline structures (thin film and bulk). This was confirmed with micro-Raman spectroscopy measurements (Fig. 6) where the bands 1154 cm^{-1} and 1158 cm^{-1} corresponds to formation of two crystalline structures. The band at 1154 cm^{-1} is highly related to carrier transport of pentacene films, because it reflects the coupling between molecules of pentacene. Similar results were obtained by including of PMMA layer under pentacene layer [4].

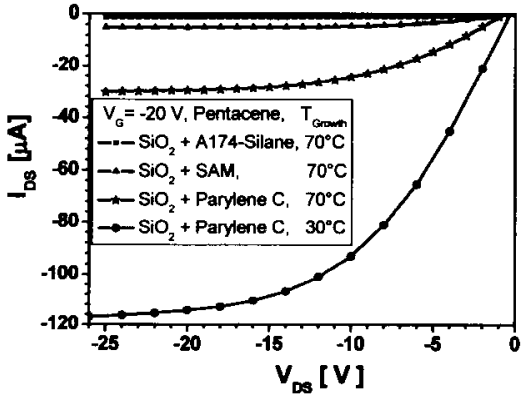

Fig. 1. OFET output characteristic for different dielectrics at constant V_G.

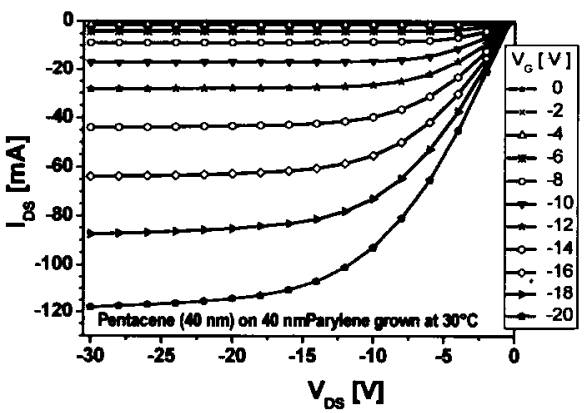

Fig. 2. OFET output characteristics for pentacene grown on parylene dielectric.

Fig. 3. AFM image (3 × 3 μm) of thin 3 nm pentacene layer grown at 30°C on parylene layer.

Fig. 4. AFM image (3 × 3 μm) of thin 3 nm pentacene layer grown at 70°C on parylene layer.

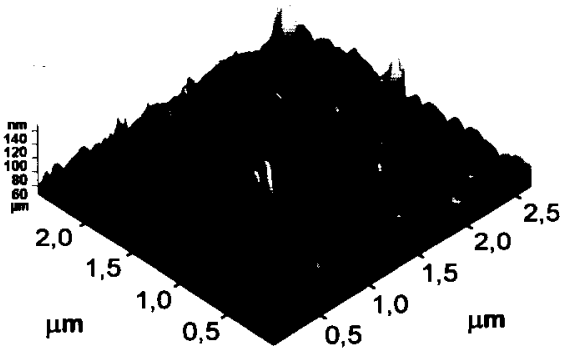

Fig. 5. 3D AFM image of 40 nm pentacene layer grown at 30°C on parylene layer.

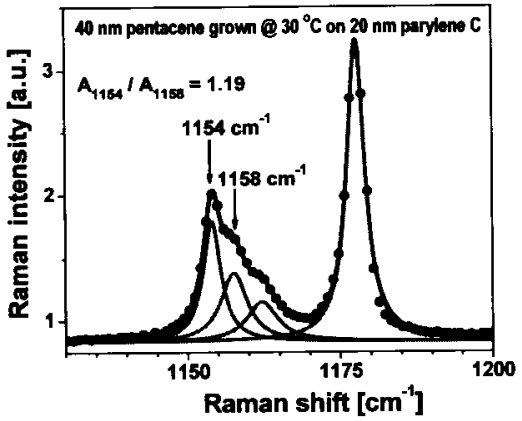

Fig. 6. 40 nm pentacene grown at 30°C on parylene Raman spectrum.

In summary, the measured results confirmed that the gate dielectric layer at the pentacene/dielectric interface is essential origins, which considerably influenced the carrier transport phenomena and achievable drain current of pentacene OFETs.

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