ACCURATE TIME MEASURE ON SPARTAN 3E FPGA

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1. Introduction

Accurate time measure is often used in various industrial branches (nuclear physic, hight frequency...) On this purpose Time to Digital Converter (TDC) well known method is often used. This method is usually implemented to ASIC [4] or FPGA [1-3] circuits. However development and subsequently implementation TDC to ASIC circuit (main in small series) is expensive and time-consuming. Nowadays using FPGA circuits is better solution. Modern FPGA provide except basic gate array also carry chain. Construction of this carry chain is appropriate on accurate time measure implementation. This article is focused on design, realization and implementation TDC in FPGA Spartan 3E with carry chain.

2. Principe of measurement

Overall simply (coarse) time measure of Δt in digital circuits is defined as counting of clock pulse till measured signal is in the requested state (for example log. 1). After measurements we multiply numbers of impulse (J) with length of one clock period (Tclk) and we get estimated coarse time (Δtc).

$$\Delta t = \Delta tc = J * Tclk \tag{1}$$

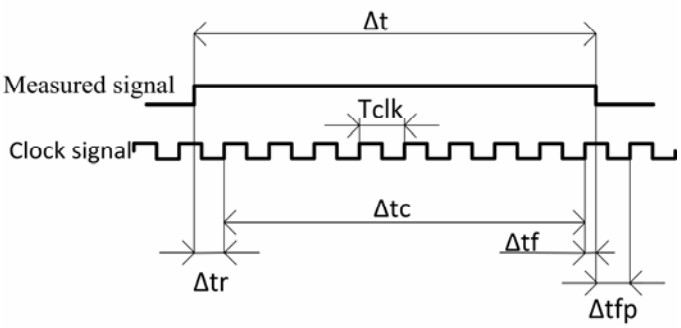

Fig.1: *Principe of accurate measurement*

As we can see on the Fig. 1 this method does not calculate with time intervals Δtr and Δtf . Δtr is a time interval between rising edge of the measured signal and rising edge of clock signal. And Δtf is time interval between rising edge of the last clock signal and falling edge of measured signal. If we calculate with these time intervals, equation (1) change to equation

$$\Delta t = \Delta tc + \Delta tr + \Delta tf \tag{2}$$

3. FPGA Spartan 3E and Carry chain

In general nowadays FPGA contains a lot of dedicate high-speed carry chain which are created by combining neighbor logical elements together through fast lines. These dedicate carry chain are in general used to implement arithmetic function as are fast adders, counters and comparators. Important feature of carry chain is that each element connected in chain has small predefined time delay (β). On the Fig. 2 we can see part of carry chain created in Spartan 3E. As delay elements are here used multiplexers from SLICEL.

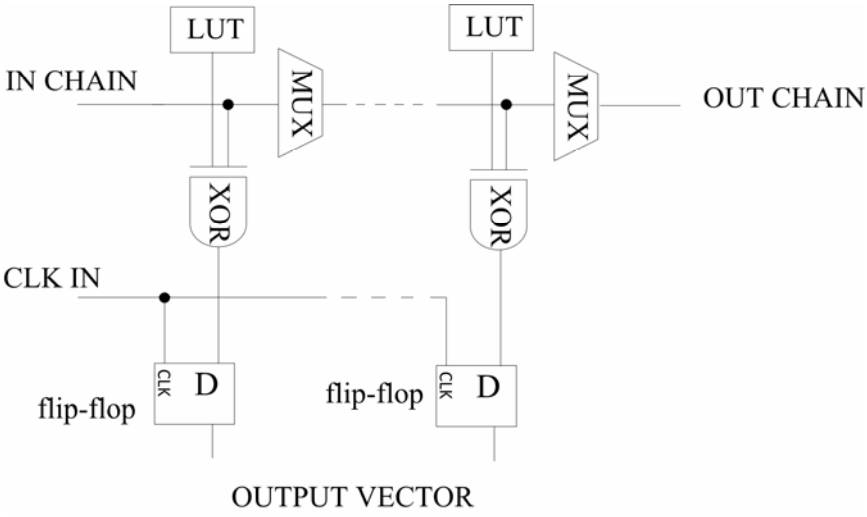

Fig.2: *Simply Carry Chain*

At the beginning of carry chain is connected measured signal. This signal gradually passes through delay elements. Between two delays elements is connected D circuit involves as flip-flop. As measured signal is propagated through carry chain, leaved behind itself change values on D flip-flop inputs. With the advent of the rising edge of clock signal are inputs of D flip-flops transferred to outputs. As we can see on Fig. 3 output of carry chain is forty bit vector whose part is inverted after rising edge. Number of inverted bits (ic) multiplied by delay of one carry chain element (β) is time interval Δtr

$$\Delta tr = \beta * ic \tag{3}$$

At falling edge we don't directly measure parameter Δtf , but time interval between falling edge of measured signal and first rising edge of clock signal Δtfp (Fig. 1). This time value we must subtracted from length of one clock signal period (Tclk)

$$\Delta tf = Tclk - \Delta tfp = Tclk - (\beta * ic) \tag{4}$$

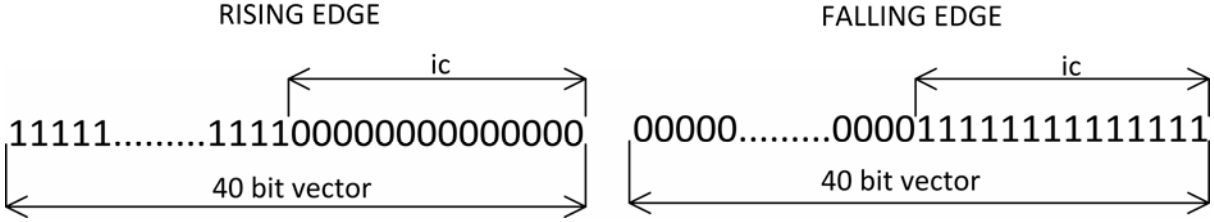

Fig.3: *Carry Chain output vector*

In our application we used 250MHz clock signal. Length of carry chain must be sufficient, that sum of delays from delays elements cover whole period of clock signal. (in our case is one period 4ns). From measurements we get, that we need forty SLICEL blocks to cover one clock period. These blocks are connected with fast lines, so delay from connection is minimal.

4. Measuring apparatus

On the Fig. 4 is measuring system which we used to validation of carry chain. At the beginning of whole system is Digital Clock Manager (DCM) which generates several frequencies. The reference frequency is 250 MHz. Second 300MHz frequency feeds *ila*, *icon* blocks and *impulse generator* block. Third low clock frequency feeds *buttons block*. Impulse generator serve to generate test impulses. 300MHz frequency ensures that rising edge and falling edge of test impulses never been generate at the same time as rising and falling edge of reference clock signal (phase shift between test impulse and reference clock). This phase shift ensures that Δtr and Δtf never been zero. Since we used only one carry chain to measure Δtr and Δtf value and these values are stored in carry chain output vector only during one clock period, we had to save these values to memory elements. In our case these elements are D circuits involved as latchs. Since carry chain output vector is forty bit vector consist from a number of successive zeros and equally a number of successive ones this vector is converted to binary value in *convert* block. These binary values are stored in internal RAM. For counting of Δtc we used simply counter whose result is also stored to RAM. For the displaying of the results we used program ChipScope. This program can choose from FPGA with implemented algorithm selected signals and display their value. PC communicates with FPGA across JTAG. Into our design we implemented *ila* and *icon* blocks. First block collects informations (values) from signal and second one controls communication between FPGA and PC. *Ila* have to be feed with 300MHz frequency. With this frequency we determine how often will be data renewed.

5. Measurement and Results

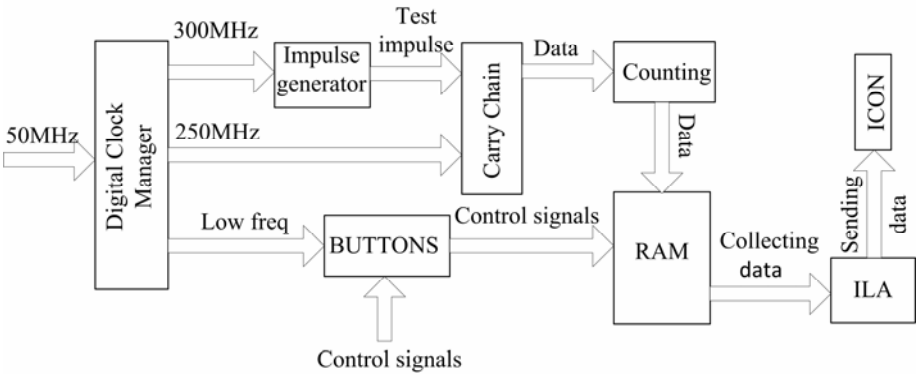

Fig.4: *Measuring apparatus*

On the Tab. 1 we can see our results. At the first measurement we generate three successive impulses. These impulses have same length but each impulse has different Δtr and Δtf (phase shift against the clock). We measure this Δtr and Δtf. Then we generate another impulses and repeated this measurement several times. From results we have received a variance of Δtr and Δtf. In our case variance Δtr or Δtf never been greater as 300 ps. This variances we added with Δtc (coarse time) and we have received variance of calculated length of test impulse. This measurement we repeat for several different impulse lengths with

different Δtr and Δtf. As we can see on the Tab. 1 main disadvantage of our measurements is, that in all case is calculated impulse length higher that real impulse length. Reason of this problem can be variance of Δtr and Δtf (and sum of these variances) or wrong implementation of carry chain to FPGA.

Measure.	**Test impulse length (ps)**	**Δtr**	**Variance Δtr** (ns)		**Δtf**	**Variance Δtf** (ns)		**Δtc** (ns)	**Calculated length of Test impulse (ps)**	
			from	to		from	to		from	to
1	36.6666	1	1.6	1.9	1	3.2	3.3	32	36.9	37.1
		2	0.2	0.3	2	3.4	3.5	32	36.7	36.8
		3	3	3.1	3	1.9	2	32	37	37
2	39.9999	1	0.2	0.3	1	3.5	3.9	36	39.8	40.2
		2	3	3.1	2	1.3	1.3	36	40.3	40.4
		3	1.5	1.6	3	2.6	2.8	36	40.2	40.3
3	43.3333	1	1.5	1.7	1	1.9	2	40	43.5	43.6
		2	0.3	0.4	2	3.2	3.3	40	43.5	43.6
		3	2.9	3	3	0.6	0.7	10	43.5	43.6
4	46.6666	1	0.2	0.3	1	2.6	2.7	44	46.9	46.9
		2	0.1	0.3	2	2.6	2.8	44	46.7	70.1
		3	2.7	2.9	3	3.9	3.9	40	46.6	46.8
5	49.9999	1	2.8	3	1	0.6	0.9	44	50	50.2
		2	1.5	1.6	2	0.5	0.8	48	50	50.3
		3	0.1	0.3	3	1.8	2	48	50	50.3

Tab. 1. *Results*

6. Acknowledgements

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