EFFECT OF CURRENT LEVELS ON THE MEMORY HYSTERESIS BEHAVIOUR OF MNOS AND SONOS STRUCTURES

Zsolt J. Horváth, Károly Zs. Molnár, Péter Turmezei, and Balázs Kovács

Óbuda University, Kandó Kálmán Faculty of Electrical Engineering,
Institute of Microelectronics and Technology, Budapest, Hungary
E-mail: horvath.zsolt@kvk.uni-obuda.hu

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1. Introduction

In a recent work the effect of layer thicknesses on the memory hysteresis behaviour of MNOS (metal-nitride-oxide-semiconductor) and SONOS (silicon-oxide-nitride-oxide-silicon) non-volatile memory structures was studied by computer simulation [1]. The main goal of the simulations was to understand our earlier experimental results [2-4]. The effect of the oxide and nitride thickness as well as the depth of charge centroid was studied. It was concluded that the optimal oxide thickness is about 2 nm, in agreement with our experimental results [2]. The decrease of nitride thickness decreased the efficiency of the injected charge. The charging behaviour deteriorated monotonically with increasing depth of charge centroid.

These dependences are connected to different potential distribution through the structure for different layer thicknesses and depth of charge centroid. The potential distribution affects the currents flowing through the oxide and nitride layers, and so the injected and captured charge. Currents flowing through the oxide and nitride layers play a key role in the charging behaviour of MNOS and SONOS structures. It seems expedient to study the effect of current levels in more details. In this paper the effects of oxide and nitride current levels on the memory hysteresis behaviour of MNOS and SONOS structures are studied by computer simulation, which is a suitable tool for this purpose.

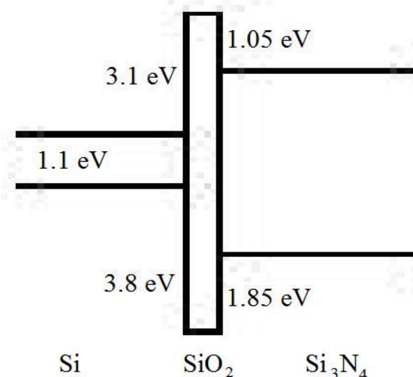

Fig. 1: *Band diagram of MNOS structures used for the calculations. The actual values of band gaps and discontinuities are taken from Ref. 5.*

2. Theoretical background

The band diagram of the MNOS structures is shown in Fig. 1 [5]. During the charging process the charge is injected from the silicon substrate through the oxide layer and it is captured by traps in the nitride layer close to the oxide/nitride interface. The captured charge yields a shift of the threshold voltage of a FET or a shift of the flat-band voltage of a

capacitor prepared on the same structure. During the charging process a part of the injected charge can be lost, as a result of a current flow through the nitride to the metal layer. The injected charge can be stored for several years.

The memory hysteresis is the dependence of the flat-band voltage of memory capacitors or of the threshold voltage of memory FETs on the amplitude of charging-recharging voltage pulses, when the amplitude is gradually increased and than decreased step by step. Such simulated hysteresis curves are presented in Fig. 2 for MNOS [1] and SONOS structures with an oxide thickness of 2 nm, equivalent nitride thickness of 30 nm, and depth of charge centroid 6 nm. The best charging behaviour was obtained for this oxide thickness in our earlier calculations [1], and these hysteresis curves are taken as reference ones in the present study.

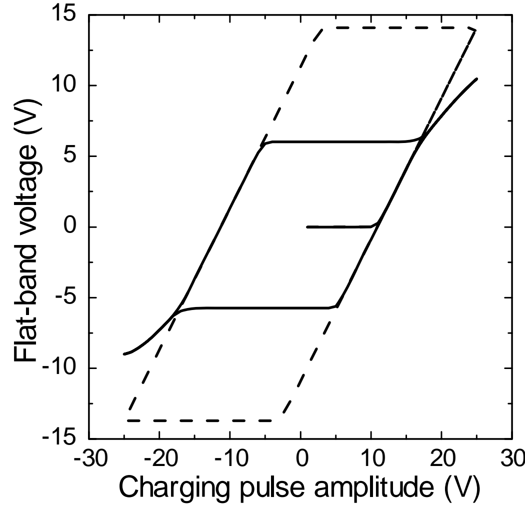

Fig. 2: *Flat-band voltage memory hysteresis curves simulated for an MNOS (solid line) and a SONOS (dashed line) structure with oxide and equivalent nitride thicknesses of 2 nm and 30 nm, respectively, and charge centroid of 6 nm.*

The memory hysteresis curves were simulated by calculating the flat-band voltage shift due to the charge injected and stored in traps in the nitride layer. The net charge captured in the nitride layer during a voltage pulse, can be calculated by the integration of the difference of the current flowing into the structure via the oxide layer and that of flowing out of the structure via the nitride layer. The current density via the oxide layer was calculated by the WKB approximation [5]:

$$J_{ox} = C_{FN} E_{ox}^2 P \tag{1}$$

where C_{FN} is a constant, E_{ox} the electric field in the oxide, and P the tunneling probability via the potential barrier. For our earlier study a C_{FN} value of $2.2\text{x}10^{-6}$ A/V^2 was used for both the electron and hole injection [5]. The reference hysteresis curves presented in Fig. 2 are calculated using this value as well. To study the effect of oxide current level C_{FN} value was varied from $2.2\text{x}10^{-12}$ A/V^2 to 2.2 A/V^2, i.e., the reference oxide current for C_{FN} value of $2.2\text{x}10^{-6}$ A/V^2 was multiplied by factors from 10^{-6} to 10^{6}.

The expression for current through the nitride layer was obtained by experiment [6]:

$$J_n = J_{PF} + J_{EX} \tag{2}$$

where J_{PF} is the Poole-Frenkel current:

$$J_{PF} = C_{PF1} \cdot E_n \cdot \exp\left(C_{PF2} \cdot \sqrt{E_n}\right) \tag{3}$$

Here C_{PF1} and C_{PF2} are parameters evaluated from our experiments (which depend on the insulator properties) and E_n is the electric field in the nitride layer between the charge centroid and metal. J_{EX} is an exponential excess current density obtained at low voltages [6]:

$$J_{EX} = C_{EX1} \cdot \exp(C_{EX2} \cdot E_n) \qquad (4)$$

where C_{EX1} and C_{EX2} are parameters evaluated from our experiments [8].

For our earlier study a C_{PF1} value of 8×10^{-26} A/Vcm was used for both charging pulse polarities [5]. To study the effect of nitride current level C_{PF1} value was changed from 8×10^{-30} A/Vcm to 8×10^{-23} A/Vcm, i.e., the reference nitride current was multiplied by factors from 10^{-4} to 10^{3}. It was observed during simulations that the excess current J_{EX} had not influence the hysteresis curves, so its value was taken zero during this study. In the case of SONOS structures the current flowing out from the structure is blocked by the top oxide layer, so zero current transport was considered via the nitiride layer.

The details of integration is described elsewhere [1]. The hysteresis curves were begun to be calculated from zero pulse amplitude and zero flat-band voltage. For the simulation of hysteresis curves the voltage pulse amplitude was increased or decreased by 1 V step by step. The pulse width used for simulations was 10 ms.

The actual barrier height values presented in Fig. 1 were taken from Ref. [5]. For both the electron and hole effective masses $m^*=0.42m_0$ was used [5], where m_0 is the free electron mass. No image force lowering and band bending at the silicon surface were considered.

3. Results and discussion

The hysteresis curve can be characterized by its height and width (see Fig. 2). The height is connected to the maximum charge that can be injected and stored in the structure, while the width is related to the electric field accuring in the oxide layer at the end of the charging pulse. This value is considered as a threshold oxide field necessary to the charge injection at a given charging pulse duration [7]. The width of hysteresis curve depends on the oxide current only, while its height is influenced by the nitride current, which yields the loss of a part of injected charge. This can be seen in Fig. 2, where the width of hysteresis is the same for both the MNOS and SONOS structure with the same equivalent thicknesses, but the height is different due to different current via the nitride layer.

The effect of the oxide current level on the width of hysteresis curve can be seen in Fig. 3. The width of the hysteresis curve increased with decreasing oxide current level, while it decreased with increasing oxide current. That means higher voltage pulse amplitudes are required for charge injection, if the oxide current level is reduced.

The height of hysteresis curves behaved in an opposite way for MNOS structures, it decreased with decreasing and increased with increasing oxide current (see Fig. 3). As no charge loss has been considered in SONOS structures, the height of hysteresis curves did not depend on oxide current.

For MNOS structures considering a multiplication factor of 10^{-4}, the hysteresis curve became small. For multiplication factor of 10^{-6} the hysteresis curve changed even its direction, positive charging pulse yielded negative flat-band voltage and *vice versa.* In this case the oxide current is lower than the nitride current, when the charging pulse is applied. Such a situation occurs in practice for thin nitride layers, if the charge is injected from the metal side. For SONOS structures the hysteresis become wider with decreasing oxide current level at low oxide currents as well.

The effect of nitride current level on the memory hysteresis behaviour can also be seen in Fig. 3. The curves are calculated for the reference oxide current. The width of hysteresis did not depend on the level of nitride current, its value was the same as in the

reference case for both MNOS and SONOS structures. For MNOS structures the height of the hysteresis decreased linearly with the logarithm of nitride current, as it can be seen in Fig. 3.

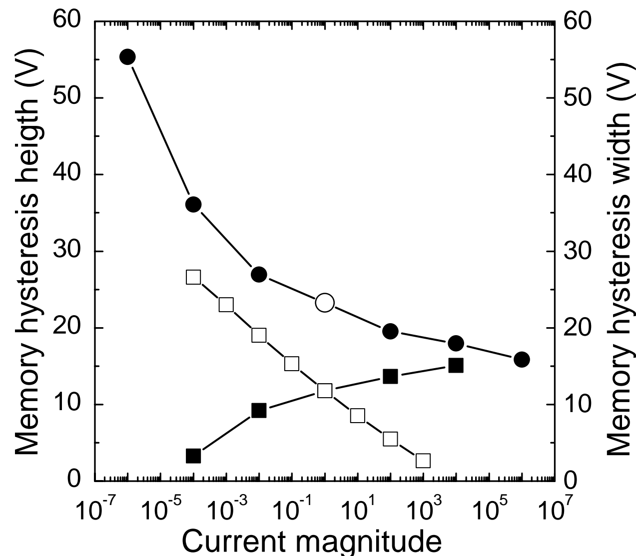

Fig.3: *The height of hysteresis curves simulated for MNOS structures as a function of multiplication factor of oxide (solid symbols) or nitride (open symbols) current level, and the widht (circles) of memory hysteresis curves simulated for both MNOS and SONOS structures as a function of multiplication factor of oxide current level.*

4. Summary

MNOS and SONOS memory hysteresis curves have been calculated. The effect of the oxide and nitride current levels has been studied. It has been obtained that the memory hysteresis width depends strongly on the oxide current level, in particular at low current levels. If the oxide current is close to the nitride current, the flat-band voltage shift is low. If the oxide current is lower than the nitride current, the hysteresis curve changes its direction.

The nitride current level affects the hysteresis height only due to charge loss via the nitride layer. In MNOS structures the height of the simulated hysteresis curves decreased linearly with the logarithm of nitride current.

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