THE EFFECTIVENESS OF DACTYL ALPHABET RECOGNITION OF NEURAL NETWORK WITH NEW ARCHITECTURE

Roman Záluský[1], Daniela Ďuračková[1], Vladimír Sedlák[1]

[1] Slovak University of Technology in Bratislava, Faculty of Electrical Engineering and Information Technology, Ilkovičova 3, 812 19 Bratislava, Slovakia

E-mail: roman.zalusky@stuba.sk

Received 20 April 2012; accepted 27 April 2012.

1. Introduction

Calculation of output activity of huge number of neurons is very demanding on the computer performance, so this implementation leads to a slower neural network compared to a hardware network implemented on the chip. Hardware implementation offers parallel data processing and therefore, the calculation of such a network is very fast. Artificial neuron itself is a complex element, which includes the operations of multiplication, sum and non-linear functions. In the commonly used data formats and standard circuits to implement the basic operations, only a small number of neurons can be feasibly implemented on the chip. Therefore, an effort to design a new neural network architecture that would use neurons working with operations could significantly help to reduce their complexity. This would also ensure less chip area overhead and therefore, much larger number of neurons on the chip could be implemented. The character recognition of Dactyl alphabet is presented, and the achieved results as well as the main advantages are discussed.

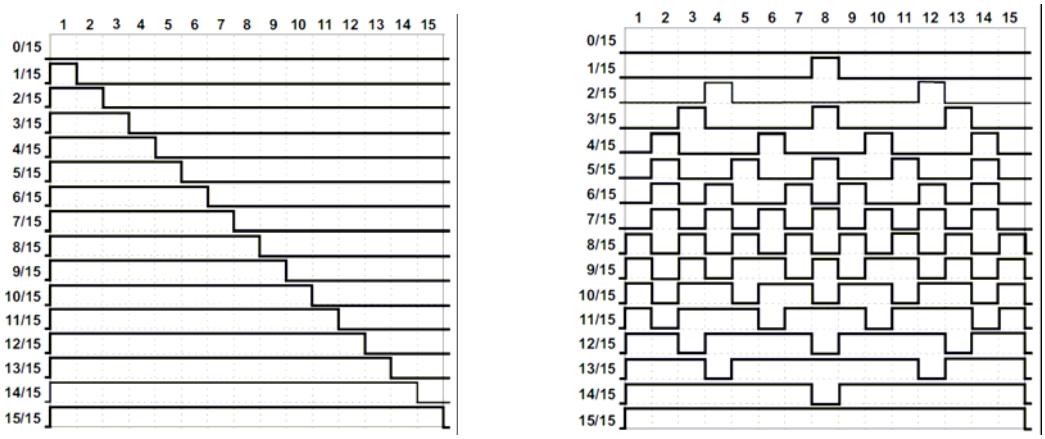
2. Equations

Some systems are very difficult to describe, or are so complex that their description is almost impossible. If we have input data and the required outputs, it is possible to approximate the response of the system. As universal approximators are widely used artificial neural networks that are trained on a given problem. Basic principles of neural networks are referred in [1–4].

The main disadvantage of neural networks working with integers as well as with floating-point numbers is high complexity of the units performing mathematical operations. Therefore, we developed a new method for serial multiplication using simple AND gates. In the proposed method of serial multiplication, the potential of the neuron is calculated in one step, because the operations of multiplication and summation are performed simultaneously. This brings a significant simplification of the neuron circuitry resulting in less area overhead. The method of multiplication using AND gate is based on subsequent multiplication of two numbers bit by bit using a simple 2-input AND gate. Numbers are always in the interval <0; 1>, because a given number is part of the specified range. This means that by two 4-bit numbers it is possible to express 16 values. Therefore, a given number will be the n-th of this value. For example, number 5 would be 5/15. We will refer to the operations of multiplication symbol as ○ (Eq. 1). Multiplication operation is performed over a time interval called "time window". Length of the time window is defined as the maximum value, which the number can take. To perform the product of n-bit numbers, *a* and *b* are the lengths of the time window 2^{n-1} time units. For the proper function of multiplication, it is necessary that coefficients are encoded in time. One number has to be encoded in the time from the beginning of the time window (Fig.1a). The other number has to be encoded in the time

symmetrically around the center of the time window as shown in Fig.1b. In the multiplication process, it does not matter, which number is encoded one way or another but both numbers must be encoded in different ways. The operation of multiplication is implemented by gateing encoded numbers a and b of the individual moments of time window. The product of multiplication is spread over time. The final result of multiplication is count of the ones in the time window. This multiplication has an effect of natural rounding. In order to be able to work also with negative values, it is necessary to extend the numbers a and b with the signs a_s and b_s. Sign of result y_s is then calculated using the logic function XOR. This special multiplication is used to calculate the output activities of neuron and in the learning algorithm.

$$y = a \circ b \tag{1}$$



a b

Fig. 1: *Encoding the number:* a) *from the beginning of time window*

b) *symmetrically around the center of the time window*

3. Experimental part

We have tested the novel architecture of a feed-forward neural network for recognition of Dactyl alphabet characters. In this application, the neural network assists in learning a sign language by the recognition of a correctly shown character (sign) of Dactyl alphabet. Dactyl alphabet, which we used, contains 36 characters. To capture the finger positions sensory glove 5DT Data Glove Ultra has been used [5]. There are 14 optical sensors spread over the glove surface. Between each pair of fingers, there is a sensor that scans the diversion of these fingers. Additionally, each finger has two sensors, which scan its bending. Since the glove consists of no sensor that would scan the position of the wrist, we added this control in our software, so the position of the wrist can be entered through this control. The sensory glove is connected to a computer via a classical serial port, USB or wireless interface. In our case, the sensory glove was connected through the USB interface. The developed software Dactyl Teacher has three types of neural networks implemented. The new architecture of feed-forward neural network, the feed-forward neural network working with floating-point numbers, and the perceptron. Neural networks have 20 inputs, where 14 inputs are outputs from the sensory glove and 6 inputs represent the wirst position. We can create the neural network with different topologies by set the number of hidden layers and the number of hidden neurons in each hidden layer. The neural network with the novel

architecture is trained by the modified error back propagation algorithm. After the learning phase is finished, it is possible to generate VHDL files of the adapted neural network.

We have verified the correct function of the new feed-forward neural network architecture on recognition of characters of Dactyl alphabet. Dactyl alphabet, which we used, contains 36 characters. The recognition effectiveness of dactyl alphabet for three types of neural network (Perceptron, FFNN with float numbers and the novel architecture of FFNN) has been evaluated. We increased the number of training objects for each character in Dactyl alphabet while the neural network was still able to recognize all considered characters correctly. The obtained results are shown in Fig. 2. Perceptron type of neural network needed for recognizing all 36 characters the training set of 6 training objects for each character. Neural network of the proposed novel architecture was able to recognize all the characters trained by the training set that contains three objects for each character. On the other hand, only two training objects were used in the training phase for the full recognition of all characters by a feed-forward neural network operating with float numbers.

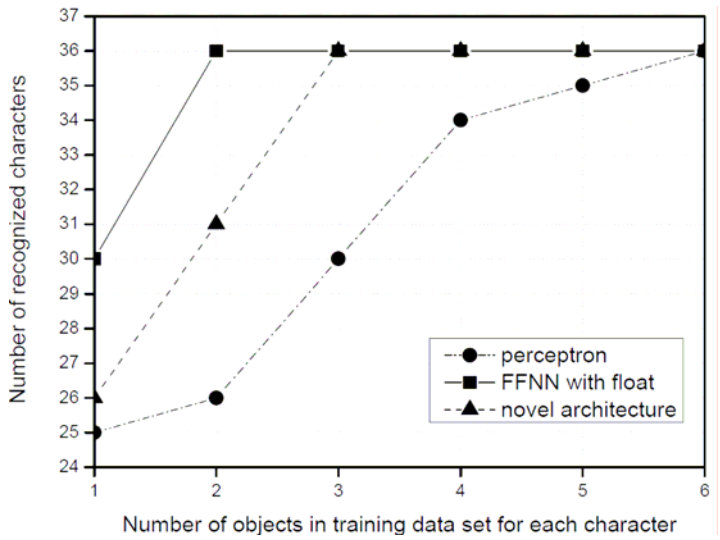


Fig. 2: *The effectiveness of Dactyl alphabet correct recognition in dependency on the number of training objects for each character.*

Finally, the calculation time t_{calc} of output activities of the neural networks was investigated. In this experiment, all neural networks contain two hidden layers. The values of the maximum frequency f_{max} of clock signal were obtained through synthesis of VHDL description of each architecture. The new architecture of a digital neural network was compared to neural networks working with integers and floating-point numbers. In case of neurons working with integers, we realized two different solutions, one working with serial multipliers and the other using parallel multipliers. Neurons working with floating-point numbers use Microfloat format [6], since it is the simplest FP format. For architectures working with combinational circuits, the delay of the combinational logic t_{comb} was measured and evaluated from the synthesis. In Table 1, results for the maximum frequency, the logic delay, and the calculation time of output activities for each neural network are presented. The fastest neural network is a network operating with integers using parallel multiplier, which uses only combinational circuits. The neural network operating with floating-point numbers exhibits about 6 times longer calculation time. This is mainly due to the feedback circuitry necessary for adjusting mantis and exponents. Finally, the novel NN architecture proposed in this work can operate at the maximum frequency of 37,477 MHz, which is about half the frequency achieved for the neural network operating with integers using serial multipliers. At

this frequency, the length of time window is about 400 ns. Thus the computation time of output activities for the non-optimized and the optimized neural network takes 1610 ns and 1200 ns, respectively.

Tab. 1. Comparison of computation time of neural networks with two hidden layers.

Architecture	f_{max} [MHz]	t_{comb} [ns]	t_{calc} [ns]
Serial integer	79.051	101.74	405.34
Parallel integer	-	124.9	124.9
Float	-	821.54	821.54
new non-optimized	37.477	-	1609.8
new optimized	37.477	-	1200.7

4. Conclusion

A novel architecture of a digital neuron, which uses the special multiplication by AND gate has been designed. The aim was to achieve the smallest chip area consumption in hardware implementation. The designed feed-forward neural network was used for character recognition of Dactyl alphabet, and its efficiency in solving this task was evaluated. Dactyl alphabet gestures were captured through a special sensoric glove 5DT Data glove. Neural network of the proposed novel architecture was able to recognize all the characters trained by the training set that contains three objects for each character. The computation time of the new architecture of a digital neural network was compared to neural networks working with integers and floating-point numbers. Thus the computation time of output activities for the non-optimized and the optimized neural network takes 1610 ns and 1200 ns, respectively.

Acknowledgement

This work has been supported by the project "Support of the Centre of Excellence for Smart Technology, Systems and Services II", ITMS Code 26 24 01 20 005, and by projects VEGA 1/0987/12 sponsored by Ministry of Education of the Slovak Republic.

References:

[1] V. Kvasnička, Ľ. Beňušková, I. Farkaš, A. Kráľ, J. Pospíchal and P. Tiňo: Introduction into the neural networks (In Slovak), IRIS, Bratislava, (1997).

[2] Sinčák and G. Andrejková: Neural Networks (The engineering methodology) part 1. (In Slovak), Elfa s.r.o., Košice (1996).

[3] C. R. Alavala: *Logic and Neural Networks: Basic concepts and applications*, New Age Publications , (2007).

[4] Theodoridis and K. Koutroumbas: Pattern Recognition, Academic Press, Boston, (2009).

[5] Fifth Dimension Technologies, 5DT Data Glove 14 Ultra, 25.11.2011, http://www.5dt.com/products/pdataglove14.html

[6] W. Kahan: *IEEE standard 754 for Binary Floating-Point Arithmetic,* Elect. Eng. and Computer Science, (1997).