DETERMINING OF THE FAILURE MECHANISM DURING UIS TEST COMBINING SINGLE AND MULTIPULSE UIS TEST

Juraj Marek, Daniel Donoval, Aleš Chvála, Patrik Pribytný, Marián Molnár

Institute of Electronics and Photonics, Slovak University of Technology,
Ilkovičova 3, 812 19 Bratislava, Slovakia,
E-mail: juraj.marek@stuba.sk

Received 09 May 2012; accepted 15 May 2012.

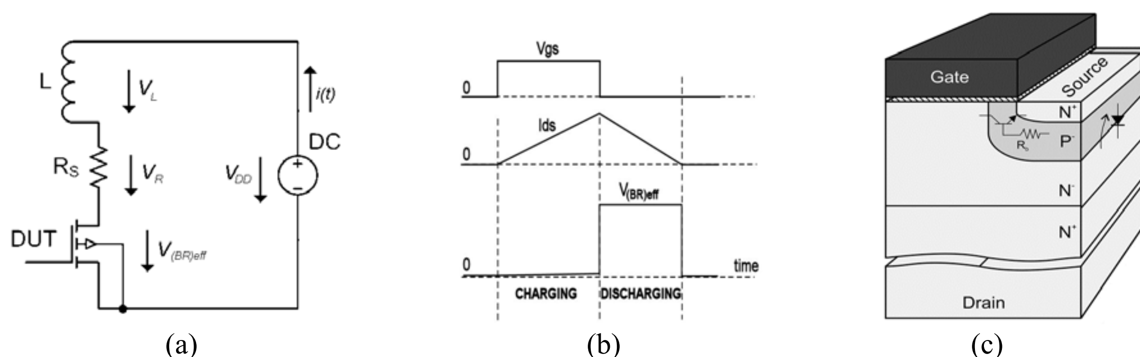
1. Introduction

The power MOSFET is a very important device used in many power-electronics applications mostly as switches, where they often have to switch high voltages and currents flowing through inductances [1]. Unclamped and parasitic inductances are the most dangerous parts in terms of switching because they can cause the most serious failures of control circuitry or destructive damage of power MOS transistor since all of the energy stored in the inductor during the on-state is dumped directly into the device during its turned off [2]. Fortunately, robust design of power MOSFETs lets them withstand certain stress levels, thus eliminating the need for expensive protection circuits, if designers carefully analyze performance parameters. An Unclamped Inductive Switching (UIS) test condition represents the harsh circuit switching operation for evaluating ruggedness of the device.

Two failure modes exist when MOSFETs are subjected to UIS. In this article, these failure mechanisms are labeled as either active or passive. The first, or active mode, results when the avalanche current forces the parasitic bipolar transistor into conduction. The second, or passive mode, results when the instantaneous chip temperature reaches a critical value [3]. At this elevated temperature, a mesoplasma forms within the parasitic npn bipolar transistor and causes catastrophic thermal runaway. In either case, the MOSFET is destroyed. From classical UIS test conception it is hard to determine which destructive mechanism plays dominant role. In our analysis we try to combine several types of UIS test to clearly determine type of destruction.

2. UIS test

Whenever current through an inductance is quickly turned off, the magnetic field induces a counter electromagnetic force (EMF) that can build up surprisingly high potentials



(a) (b) (c)

Fig. 1: (a) Simplified UIS test circuit used for measurement (b) Current and voltage waveforms of the tested device under UIS test conditions. c) Cross-section of a vertical power MOSFET structure with highlighted parasitic devices.

across the switch. Mechanical switches often have spark-suppression circuits to reduce these harmful effects that result when current is suddenly interrupted. However, when transistors are used as the switches, the full buildup of this induced potential may far exceed the rated breakdown ($V_{(BR)DSS}$) of the transistor, thus resulting in catastrophic failure. If we know the size of the inductor, the amount of current being switched, and the speed of the switch the expected potential may be easily calculated as:

$$V = L\, di/dt + V_{DD} \tag{1}$$

Where L is the inductance (H), di/dt is rate of change of current (A/s) and V_{DD} is the supply voltage (V). The classic UIS test circuit in widespread use is shown in figure 1. Using this circuit, the energy absorbed by the power MOSFET may be calculated using formula 2.

$$E_{AV} = \frac{1}{2} L I_{AV}^{2} \ , \ R_S = 0 \tag{2}$$

Reviewing the switching waveform shown in Figure 1, the gate remains on long enough to ramp the current to I_O, at which time the gate switches off, resulting in an abrupt break in the drain current. Since the magnetic field of the inductor cannot instantaneously collapse, a voltage is induced on the drain of the MOSFET in accordance with equation 1. This induced potential may easily exceed the (avalanche) breakdown voltage. During avalanche, the voltage is clamped at a value of $V_{(BR)eff}$, and the current stored in the inductor decays linearly from I_O to zero. This decay time may be determined by rearranging equation 1.

$$t_{AV} = \frac{L I_{AV}}{V_{BReff}} \tag{3}$$

3. Destruction modes

The Bipolar Excitation Effect – The "Active" Mode. The initial avalanche current at breakdown is heavily concentrated within the MOSFET's inherent Zener diode (afforded by the deep p+ well situated centrally in each cell, as shown in Figure 1c). Avalanche current concentrated in the p+ (Zener) region does not normally initiate bipolar action. As the avalanche current increases in intensity it spreads along the p/n barrier. If the avalanche currents cascading laterally through the p-doped region (pseudobase region) develop sufficient forward bias across R_B to offset V_{BE}, the normal forward base current, $+I_B$, in conjunction with the beta of the parasitic npn bipolar transistor, will result in a local breakdown voltage equal to BV_{CEO} (which is approximately half of $V_{(BR)DSS}$). The resulting mesoplasma causes thermal runaway and the destruction of the power MOSFET.

The Thermal Effect – The "Passive" Mode. During UIS, as the MOSFET is subjected to increasing energy, the internal chip temperature rises dramatically (equation 4) and is thought to generate a mesoplasma. Such mesoplasmas (regenerative heating) lead to the irreversible damage generally associated with thermal runaway.[1] The swiftness of this temperature rise, see equation (3), tends to make heat sinks irrelevant for UIS testing. During this avalanche period, as defined by equation (3), energy is dissipated in the device equation (2), resulting in a dramatic increase in chip temperature. Maximum temperature rise ΔT_M during this avalanche period was derived by Blackburn for one dimensional model [4].

$$\Delta T_M = \frac{\sqrt{2}}{3} K . I_{AV} . V_{BReff} . \sqrt{\frac{L I_{AV}}{V_{BReff}}} \text{, where } K = \frac{2}{A.\sqrt{\rho.\pi.\kappa.c}} \tag{4}$$

A is active area, ρ is density of Si, κ is thermal conductivity and c is specific heat of silicon. Blackburn assumed in his model that V_{BR} is not changing due to heating. Also thermal conductivity of silicon is assumed constant. Experiments done by Stoltenburg [5] shoved that

temperature rise in practice differs from Blackburn model. Therefore Stoltenburg derived new equation for ΔT_M :

$$\Delta T_M = \frac{\sqrt{2}}{3} K.I_{AV}.V_{BReff}.\sqrt[2.2]{\frac{LI_{AV}}{V_{BReff}}} \text{, for } \Delta T_M\text{=const} \rightarrow I_{AVcrit} \propto \sqrt[3.2]{\frac{1}{L}} \qquad (5)$$

4. Experimental results

For analysis novel locally charge balanced trench based super-junction n-channel power MOSFET was used. Samples exceed $V_{BR(DSS)}$ = 700 V, V_{GSth}= 4 V, R_{ON}= 23mΩ/cm^2 and single pulse drain-to-source avalanche energy E_{AS} = 800 mJ for L = 10mH. The maximal non-destructive energies were measured on wafer level using ITC55100 tester with combination with high current probes. Typical waveforms during test are shown on figure 2a and measured values of I_{AVcrit} for different values of inductance are shown on figure 2b. Also high temperature measurements were done using thermal chuck and two transistors set-up. Figure 2c shows avalanche current versus starting temperature for four values of inductance, ranging from 3mH to 30 mH. These data represent single-event UIS failures and further may identify maximum junction temperature T_J. For any given inductance, the avalanche failure current decreased as the starting temperature increased. The x-axis intercepts of the linear fit for each value of inductance identify maximum junction temperature. One can clearly see that with increasing inductance is also increasing value of intersection. This increase can be attributed to different mechanisms of destruction. However it is hard to distinguish dominant type of destruction. The thermal effect mode assume that destruction occur at same critical temperature (equations 4 & 5). Critical temperature of our samples was also verify using multipulse UIS test for high inductances and low currents to ensure that parasitic BJT is not excited (figure 3). The duty cycle of pulses was set at maximum to ensure that starting temperature of following pulse is higher than previous one. One can clearly see that for set up like this destruction occur at same temperature. From results shown on figure 2b and 2c we can assume that for inductances higher than 30 mH parasitic BJT is not excited and dominant mechanism of destruction is only the thermal effect (passive mode). For lower inductances the bipolar excitation effect assumes destruction at same current. Samples used in our analysis exhibit this effect for inductances lower than 1mH. For inductances in range from 1mH to 30mH combination of both effects is present. Critical value of current is higher than calculated using Blackburn or Stoltenburg formulas. This is due to the fact that destruction doesn't occur at maximum temperature (eq. 4 & 5) and approximately in the middle of avalanching period but at lower temperature and in the first third of avalanching period. One can clearly see that from comparison of measured data and plotted Blackburn or Stoltenburg formula can be determined which mechanism of destruction plays dominant

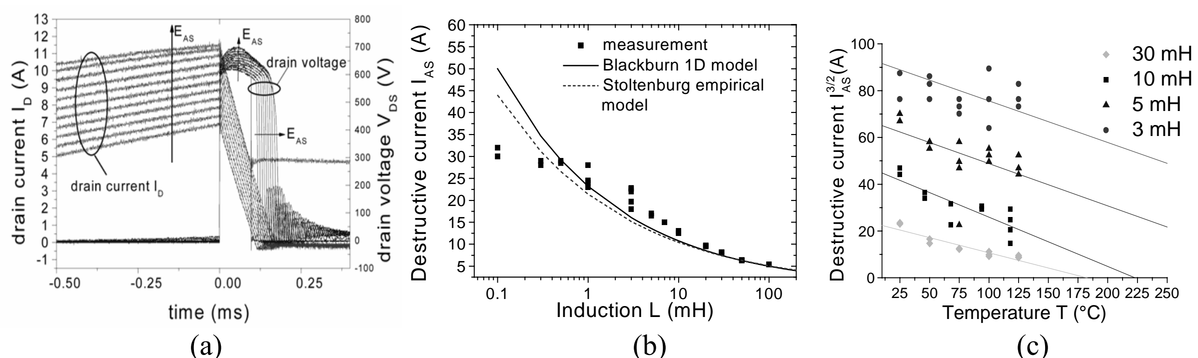


Fig. 2: (a) Typical waveforms during measurement. (b) measured values of I_{AVcrit} for different values of inductance compared with Blackburn and Stoltenburg models. (c) High temperature measurements for L = 3 – 30 mH.

role for each inductance without need of high temperature measurements.

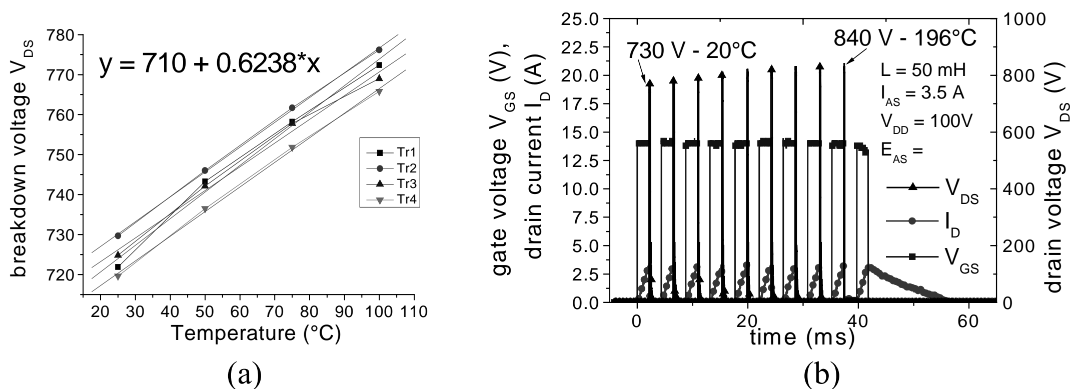


Fig. 3: (a) Temperature dependence of breakdown voltage. (b) Multipulse UIS test – determination of maximum junction temperature.

5. Conclusion

Measurements of UIS test were done on high voltage power MOSFET samples for different inductances and temperatures. We have shoved that using combination of multipulse UIS test with single shot UIS test and model derived by Blackburn can be used to exactly determine type of destruction for several inductances.

Acknowledgement

This work has been done with support of grant END (ENIAC JU No. 120214).

References:

[1] J. Roig, E. Stefanov, F. Morancho. *IEEE Trans. Electron Dev.,* **53**, 1712 (2006).
[2] K. Fischer, K. Shenai, *IEEE Trans. on Electron Dev*., **43** 1007 (1996).
[3] C. Buttay, et.al., *IEEE Power Electron. Lett,* 2, 104 (2004).
[4] D. L. Blackburn, *IEEE Power Electronics Specialists Conference,* 429 (1985),
[5] R.R.Stoltenburg, *IEEE Applied Power Electronics Conference Proceedings,* **359** (1989)