INVESTIGATION OF AMORPHOUS SILICON/CRYSTALLINE SILICON INTERFACE FOR HETEROJUNCTION SOLAR CELL APPLICATIONS

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1. Introduction

The opportunity to achieve high performance and still maintain low fabrication costs has become the motivation for extensive studies of solar cells with a-Si:H/c-Si heterojunctions. It has been shown by simulations as well as by experiments that in these structures the interface properties play a crucible role [1, 2]. To fully utilize the potential of this hybrid solar cell technology it is necessary to optimize the fabrication process of such structures to suppress recombination at the a-Si:H/c-Si interface [3, 4]. An important part in this process is the measurement of the interface defect density. There are various methods for inspection of the interface quality. The most common among them are the capacitance spectroscopy techniques. However, methods such as capacitance quasistatic diagnostics and conductance method, which offer very reliable results for MOS structures, are not applicable in investigating the heterojunction interface quality [5]. Capacitance spectroscopy in the dark at zero or slightly reverse bias, the so-called admittance spectroscopy, has been successfully applied to study the a-Si:H/c-Si interface [6]. The stepwise increase of capacitance upon increased temperature was attributed to the trapping and emission of electrons and holes by the interface defect states. The main drawback of this technique is its low sensitivity. Due to the high background c-Si space charge capacitance, the detectable defect state density begins at a value of 5×10^{12} cm^{-2} [6]. To overcome this limitation, measurement of capacitance in accumulation under AM1.5 light illumination was recently proposed [7]. The aim of this paper is to examine this method for a-Si:H(n)/c-Si(p) interface properties investigation. The sensitivity and reliability of the method is inspected using numerical simulation provided by software AFORS-HET and the practical applicability is demonstrated on a-Si:H(n)/c-Si(p) heterojunction structures with different interface conditions.

2. Experimental and simulation details

Sensitivity study of capacitance spectroscopy was made using the simulation software AHORS-HET [8]. The program solves one dimensional semiconductor equations under steady-state conditions. Furthermore, a variety of common characterization techniques have been implemented into the software, such as current-voltage (*I-V*), internal quantum efficiency (IQE), and capacitance (*C-V*, *C-T*). For simulation a simple structure with heterojunction TCO/a-Si:H(n)/c-Si(p)/Al was considered in which the thicknesses of the layers for TCO, n-layer and the crystalline silicon substrate were 80 nm, 10 nm and 500 µm, respectively. The defect states at the interface were modelled by introducing a 1 nm thick highly defective layer between amorphous and crystalline silicon layers. The layer was defined using the crystalline silicon parameters and with a constant distribution of acceptor and donor defects in the forbidden band. The front and back contacts were assumed as flat band ones to neglect the contact potential influence. The gap state densities of a-Si:H as well as other simulating parameters were set according to [9].

For experimental purposes, two series of a-Si:H(n)/c-Si(p) samples with an a-Si:H(i) passivation layer of thicknesses 5 nm (sample A5) and 10 nm (sample A10) and one without the passivation layer (sample A0) were prepared in the Laboratory of Photovoltaic Materials and Devices, TU Delft, the Netherlands. The intrinsic layer was introduced at the interface for passivation purpose, therefore it is assumed that sample A0 has a different interface quality compared to samples A5 and A10. The front square aluminium contacts with diameter 500 µm were evaporated on all samples and defined by lithography. As a back contact the whole area of evaporated aluminium was used with a thickness of 120 nm. Measurement of capacitance as a function of frequency was performed using an LCR meter AGILENT 4284A. Solar cell simulator 16S-002-300 with spectrum AM1.5 was used as a source of light.

3. Results and discussion

In Fig. 1a, numerical simulation is shown of the heterojunction capacitance of a 0.5 V forward biased a-Si:H/c-Si structures under AM1.5 illumination as a function of frequency. Various interfaces defect state values where set to clarify the impact of the interface quality. As one can see, the capacitance has a plateau at low frequencies and then decreases markedly. A significant decrease of low frequency capacitance in the plateau, C_{LF}, is observed upon the increase of the interface defect density. The explanation for this phenomenon is the nature of the diffusion capacitance, which is in this case measured. The diffusion capacitance is affected by the rearrangement of minority carrier density, which is strongly related to the recombination process at the interface. Therefore, capacitance C_{LF} reflects the conditions at the interface and can be used for quantification of its value. Since the interface recombination processes affect also the open circuit voltage of such a solar cell, it is possible to draw a direct relationship between these two parameters (Fig. 1b).

Due to the sensitivity of diffusion capacitance to the minority carries in crystalline silicon, it is not surprising that the quality of crystalline silicon as well as the back interface quality will also significantly influence the C_{LF} capacitance. The quality of the crystalline substrate is characterized by the carrier life time, τ. A strong decrease of C_{LF} is observed upon the decrease of τ (Fig. 2a.) Considering the back interface, a strong drop of C_{LF} is observed when the back surface recombination velocity S_{back} increases from 10^3 to 10^4 cm/s (Fig. 2b). It is also shown that the presented method is highly sensitive to the defect state value around the value of 10^{12} cm^{-2}, where a significant drop of capacitance can be observed for a small change of defect states (Fig. 2b).

The recombination processes in the a-Si:H(n)/c-Si(p) structure depends on the inversion properties at the interface. Strong inversion, in other words a large distance between the Fermi level and the valence band, results in a decrease of the recombination probability of minority electrons with the majority holes at the interface. Inversion at the interface depends on the conduction band offset. The dependence of capacitance C_{LF} on the conduction band offset, ΔE_C, clearly follows the link between the conduction band and the inversion at the interface (Fig. 3a). A higher value of ΔE_C results in an increase of C_{LF}, which can be attributed to a decrease of the interface recombination due to higher inversion at the interface.

The presented simulation results have shown that the low frequency capacitance is highly sensitive to the defect states at the heterojunction interface. However, to reliably determine the defect state value, one has to distinguish various influences on capacitance C_{LF}. Among them are the conduction band offset and the back surface recombination velocity that is difficult to determine. Nevertheless, a simple way for practical utilization of this capacitance diagnostics is to keep the fabrication process of either the front heterointerface or the back interface unchanged and evaluate the change at the opposite interface. In this way, the method can be used for relative quantification of interface conditions as a feedback for the fabrication process.

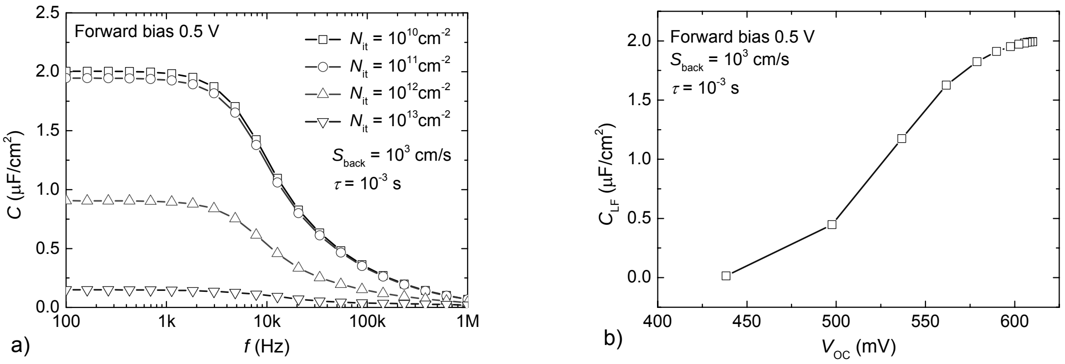

Fig. 1: *a) Simulation of capacitance at forward bias* 0.5 V *under illumination AM1.5 as a function of frequency for* a-Si:H(n)/c-Si(p) *structure with variable interface quality. b) Calculation of the relationship between the open circuit voltage and low frequency capacitance at forward bias under illumination AM1.5.*

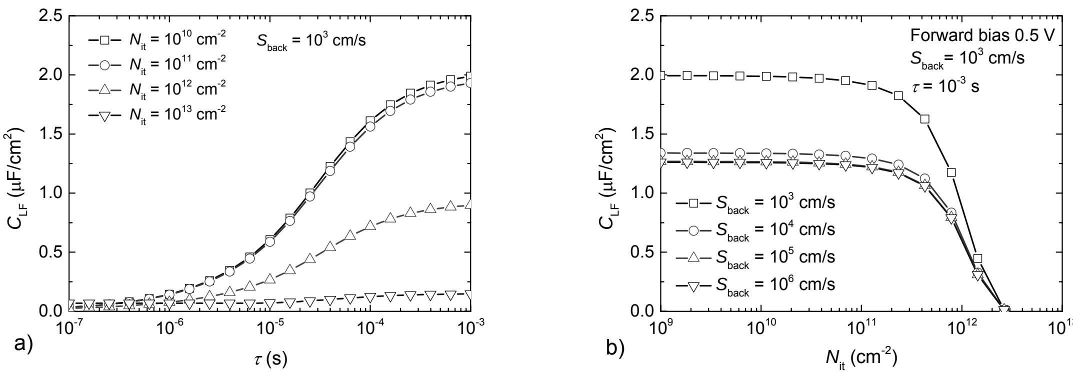

Fig. 2: *a) Simulated impact of the carrier life time in crystalline silicon on the low frequency capacitance under AM1.5 illumination at* 0.5 V *forward bias. b) Simulation of low frequency capacitance* C_{LF} *at forward bias* 0.5 V *under illumination AM1.5 as a function of interface defect density* N_{it}. *The back surface recombination velocity* S_{back} *was used as a parameter.*

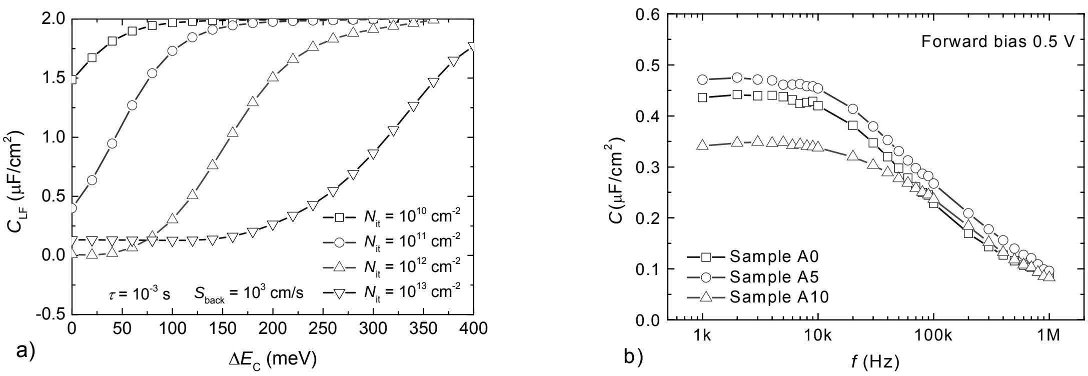

Fig. 3: *a) Simulated influence of the conduction band offset on the low frequency capacitance* C_{LF} *under AM1.5 illumination at* 0.5 V *forward bias, where various quality of the* a-Si:H(n)/c-Si:H(p) *interface was assumed. b) Measured capacitance at forward bias* 0.5 V *under illumination AM1.5 as a function of frequency for samples with various interface conditions.*

To demonstrate the applicability of the presented capacitance spectroscopy we have carried out measurements on a-Si:H(n)/c-Si(p) heterojunction structures with assumed different interface conditions. The measured capacitance as a function of frequency at forward bias 0.5 V and under illumination AM1.5 for samples A0, A5 and A10 is presented in Fig. 3b. The highest value of low frequency capacitance was measured for sample A5. The interface of this sample is passivated by a 5 nm thin intrinsic layer. The higher value of C_{LF} in this sample compared to the sample without the passivation layer, A0, underlines the decrease of the defect density when a passivation layer of intrinsic amorphous silicon is used. The lowest value of C_{LF} is observed for sample A10, where a 10 nm intrinsic amorphous passivation layer is used. To explain this behaviour we have to take into account the band offset of this structure. The coplanar conductance measurement has shown a drop of the conduction band offset when a thicker intrinsic layer is introduced at the interface [5]. In the case of sample A5 we measured the band offset ΔE_C=165 meV whereas for sample A10 the band offset dropped to 140 meV. Simulation gives evidence on a strong impact of the conduction band offset on C_{LF} (Fig. 3a). When we assume similar passivation properties of the interface for samples with 10 nm and 5 nm thick passivation layers, we can assign the low value of measured C_{LF} in sample A10 to the decrease in the conduction band offset.

4. Conclusion

The crucible role of a-Si:H/c-Si heterointerface conditions for solar cells applications underlines the requirement to have a methodology for measurement of the interface defect states. Measurement of the accumulation capacitance under illumination offers sufficient sensitivity to describe this parameter. Using simulation, we have shown various limitations and influences which has to be taken into account when this method is applied. Measurements carried out on three series of a-Si:H(n)/c-Si(p) solar structures have shown different capacitance responses. The results are in accordance with simulated expectations and assumed interface conditions at the interface of the samples studied.

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