COMPARATIVE STUDY OF InAlN/GaN HFETs WITH AND WITHOUT THERMAL OXIDIZED InAlN OF DIFFERENT COMPOSITIONS

P. Kordoš[1,2], R. Stoklas[2], K. Čičo[2], M. Mikulics[3]

[1]Institute of Electronics and Photonics, FEEI STU Bratislava, [2]Institute of Electrical Engineering, SAS Bratislava, Slovakia, [3]Peter Grünberg Institute (PGI-9), Research Centre Jülich, Germany

E-mail: peter.kordos@savba.sk

Received 30 April 2012; accepted 09 May 2012.

1. Introduction

The main advantages of InAlN/GaN material structure should be that InAlN with 17–18 % of InN can be grown lattice matched to GaN. This should led to reduced or eliminated surface related current collapse, i.e. better high-frequency performance, as the piezoelectric polarization charge is eliminated [1]. However, the best microwave performance (f_T/f_{max} of 205/220 GHz) has been reported using tensely strained InAlN (13.4 % of InN) [2]. Recently we have shown that InAlN/GaN heterostructures with tensely strained InAlN can be useful for high-frequency HFETs and with compressively strained InAlN for enhancement mode GaN-based devices [3]. On the other hand, it is well known that AlGaN/GaN metal-oxide-semiconductor HFETs (MOSHFETs) show better microwave power performance than simple HFETs [4]. However, less is reported on InAlN/GaN MOSHFETs. Thermal oxidation of InAlN surface as a possible preparation method of thin gate insulator and/or surface passivation is under systematic study since recently [5-7]. Oxidation process is found to be diffusion limited, similarly as well known for thermal oxidation of Si. Unfortunately, a decrease of the channel charge density due to the oxidation process is observed [5]. Thus, detailed investigations of InAlN oxidation on the device properties are needed.

We present a comparative study related to the properties of the InAlN/GaN heterostructures and devices with non-oxidized and oxidized InAlN of different compositions (13, 17 and 21 % of InN). Static and pulsed current-voltage (I–V) characteristics as well as frequency dependent capacitance (C–V) measurements were performed on devices prepared. From the results described below it follows that the thermal oxidization of InAlN increases the density of trap states, independently on the InAlN composition.

2. Experimental

The InAlN/GaN heterostructures used in this study were grown by metal-organic vapor phase epitaxy on Si(111) substrate. They consisted of ~2 μm GaN insulating buffer layer followed by a 1 nm AlN spacer layer and a 10 nm InAlN barrier layer. Heterostructures with three different compositions of the InAlN were prepared. The first one was with an InAlN nearly lattice-matched to GaN, i.e. with ~17.5 % of InN – designated as "18-type" in the next. The other two were with tensely (13% of InN) and compressively (21% of InN) strained InAlN barrier layer. Oxidation of InAlN surface was performed in pure oxygen ambient at atmospheric pressure at the temperature 750 °C for 2 min. Conventional transistor fabrication steps, known for AlGaN/GaN HFETs, were used for the device preparation. At first a multilayered Ti/Al/Ni/Au sequence for the ohmic contacts was evaporated and patterned. Afterwards, mesa isolation by ion beam etching in Ar plasma was made. The ohmic contacts were formed by rapid thermal annealing at 800 °C for 2 min in a N_2/H_2

forming gas atmosphere. Finally, Ni/Au Schottky gate contacts were patterned by electron-beam lithography. Devices with a gate length ranging between 0.5 and 2.5 μm and a gate width of 2 × 50 and 2 × 100 μm as well as large area capacitors (100×100 and 200×200 μm^2 gate contact area) were prepared. The passivated (120 nm SiN) as well as unpassivated devices were prepared from the same wafer.

3. Results and discussion

Static output characterization of the non-oxidized InAlN/GaN HFETs typically yielded *I–V* characteristics at $V_G = 0$ V as shown in Fig. 1 (dashed lines). The saturation drain current I_{DS} = 1.19, 0.84 and 0.55 A/mm was obtained for 13-, 18- and 21-type devices, respectively. This result confirms expected decrease of the sheet charge density in the channel with increased InN mole fraction in the InAlN barrier layer, as

$$I_{DS}/w_G = q \cdot n_s \cdot v_d, \tag{1}$$

where w_G is the gate width and v_d is the drift velocity of carriers. On the other hand, the saturation drain current I_{DS} = 0.94, 0.57 and 0.29 A/mm was obtained for oxidized 13-, 18- and 21-type devices, respectively (Fig. 1 – full lines). A decrease of the channel charge density due to the oxidation process is evident. The difference between the saturation drain current before and after oxidation is the same for all three types of devices, $\Delta I_{DS} \cong 0.26$ A/mm. This indicates that nearly the same density of traps, which reduced the drain current, was created during the oxidation of the structures investigated.

Relatively sharp transition from accumulation to depletion was observed for both types of structures in the measured *C–V* characteristics. The sheet charge density n_s was evaluated by an integration of the *C–V* curves in order to verify observed drain current data, considering that

$$n_s = (1/q) \cdot \int C \cdot dV_G \,. \tag{2}$$

The sheet charge density without an InAlN oxidation decreased from 2.2×10^{13} cm^{-2} for 13-type structure to 1.7×10^{13} and 1.1×10^{13} cm^{-2} for 18- and 21-type structures, respectively. These data scale well with the calculated total polarization charge as function of InAlN composition, as shown in Fig. 2. Obtained charge carrier densities (open marks) are about 75

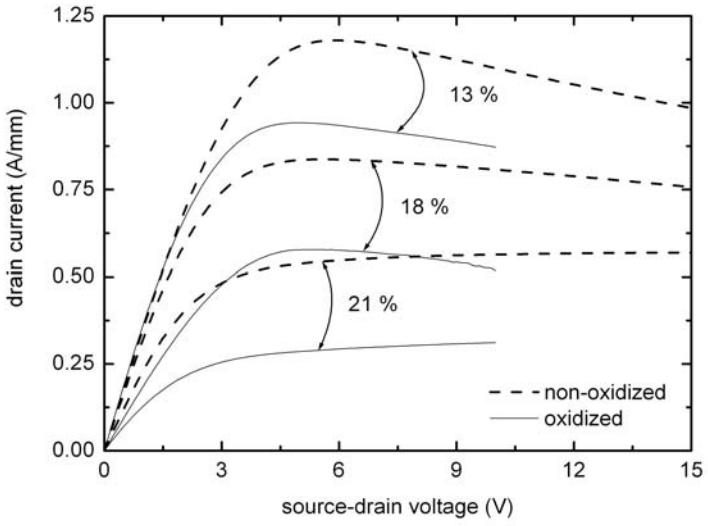

Fig.1: *Typical I–V characteristics at $V_G = 0$ V for non-oxidized (dashed lines) and oxidized (full lines) InAlN/GaN HFETs with 13, 18 and 21 % of InN in InAlN barrier layer.*

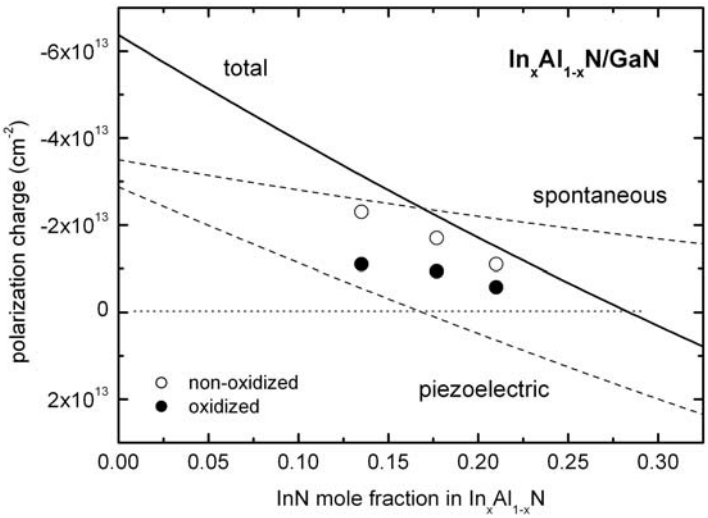

Fig.2: *Calculated polarization charge as a function of InAlN composition and experimentally evaluated sheet charge density for non-oxidized (open marks) and oxidized (full marks) InAlN/GaN structures.*

% of the theoretical values. Evaluation of oxidized structures yielded significantly lower sheet charge density, $n_s = 1.1\times10^{13}$, 0.94×10^{13} and 0.58×10^{13} cm^{-2} for 13-, 18- and 21-type devices, respectively (Fig. 2, full marks). This indicates that a relatively high density of trap states was created by the thermal oxidation of InAlN surface.

Pulsed *I–V* characteristics were measured to evaluate an effect of the oxidation on the current collapse, particularly gate lag, of the InAlN/GaN HFETs (Fig. 3). Measurements were performed using a pulse width w_p ranging between 200 ns and 1 ms. The gate was pulsed from closed to open channel conditions, i.e. from the voltage slightly below the threshold to $V_G = 2$ V. The gate lag was evaluated as a ratio of the pulsed to static drain current. A set of samples from all three types of devices was evaluated, but we could not distinguish clear difference in the gate lag for different InAlN composition. Similar result we obtained before on non- oxidized InAlN/GaN HFETs, however measured only with 1μs pulse width [3]. The

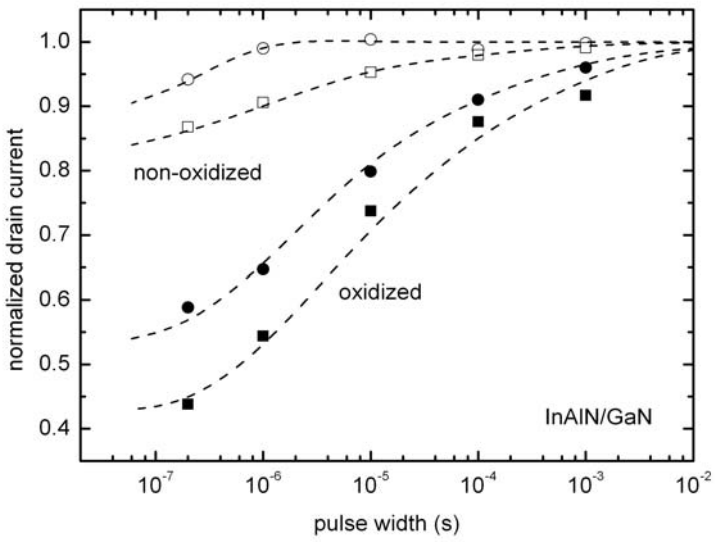

Fig.3: *Pulsed drain current normalized to corresponding static value as a function of pulse width for non-oxidized (open marks) and oxidized (full marks) InAlN/GaN HFETs.*

gate lag as a function of the pulse width for oxidized (full marks) and non-oxidized (open marks) devices is shown in Fig. 3. Two sets of data are shown for oxidized and non-oxidized devices, which represent upper and lower limit of the results obtained. The oxidized devices exhibited significant gate lag, which can be observed even at 1 ms pulse width. The gate lag increased continuously with decreased pulse width and for 200 ns pulse width the pulsed drain current is only ~50 % of the static one. It should be noted that qualitatively similar I_D vs w_p dependence as shown in Fig. 3 was reported before for unpassivated AlGaN-based HFETs [8]. This observation supports results which follow from the static *I–V* and 1 MHz *C–V* analysis given above, that the thermal oxidation of InAlN produces increased density of traps compared with that in the non-oxidized counterparts.

4. Conclusions

Properties of thermally oxidized (750 °C/2 min) InAlN/GaN heterostructures and HFETs with different InAlN composition (InN = 13, 17 and 21 %) were evaluated. The sheet charge density and thus also the drain current decreased significantly comparing to the values obtained on the particular non-oxidized counterparts. Pulsed measurements yielded very high gate lag independently on the InAlN composition, in contradiction to low gate lag observed on non-oxidized SiN passivated InAlN/GaN devices. From these results it follows that an increased density of trap states is created due to thermal oxidization of InAlN/GaN structures.

Acknowledgement

This work was financially supported by grant of Science and Technology Assistance Agency no. APVV-LPP-0162-09 and Scientific Grant Agency of the Ministry of Education of Slovak Republic and the Slovak Academy of Sciences No. VEGA-2/0098/09 and VEGA-1/0866/11.

References:

[1] J. H. Leach, M. Wu, X. Ni, X. Li, Ü. Özgür, and H. Morkoç, *Phys. Stat. Solidi* A **207**, 211 (2010).
[2] H. Sun, A. R. Alt, H. Benedickter, E. Feltin, J.-F. Carlin, M. Gonschorek, N. R. Grandjean, and C. R. Bolognesi, *IEEE Electron Device Lett*. **31**, 957 (2010).
[3] M. Mikulics, R. Stoklas, A. Dadgar, D. Gregušová, J. Novák, D. Grützmacher, A. Krost, and P. Kordoš, *Appl. Phys. Lett*. **97**, 173505 (2010).
[4] P. Kordoš, G. Heidelberger, J. Bernát, A. Fox, M. Marso, and H. Lüth, *Appl. Phys. Lett*. **87**, 143501 (2005).
[5] M. Alomari, F. Medjdoub, J.-F. Carlin, E. Feltin, N. Grandjean, A. Chuvilin, U. Kaiser, C. Gaquière, and E. Kohn, *IEEE Electron Device Lett*. **30**, 1131 (2009).
[6] J. Kováč, R. Šramatý, A. Chvála, H. Sibboni, E. Morvan, M. A. DiForte-Poisson, D. Donoval, and P. Kordoš, *Appl. Phys. Lett*. **98**, 162111 (2011).
[7] M. Eickelkamp, M. Weingarten, L. R. Khoshroo, N. Ketteniss, H. Behmenburg, M. Heuken, H. Kalisch, R. H. Jansen, and A. Vescan, *Phys. Stat. Solidi* C **8**, 2213 (2011).
[8] G. Meneghesso, F. Rampazzo, P. Kordoš, G. Verzellesi, and E. Zanoni, *IEEE Trans. Electron Devices* **53**, 2932 (2006).