ANALYSIS OF A LOW VOLTAGE VERTICAL POWER MOS TRANSISTOR FAILURE DURING UIS TEST SUPPORTED BY 2-D AND 3-D SIMULATIONS

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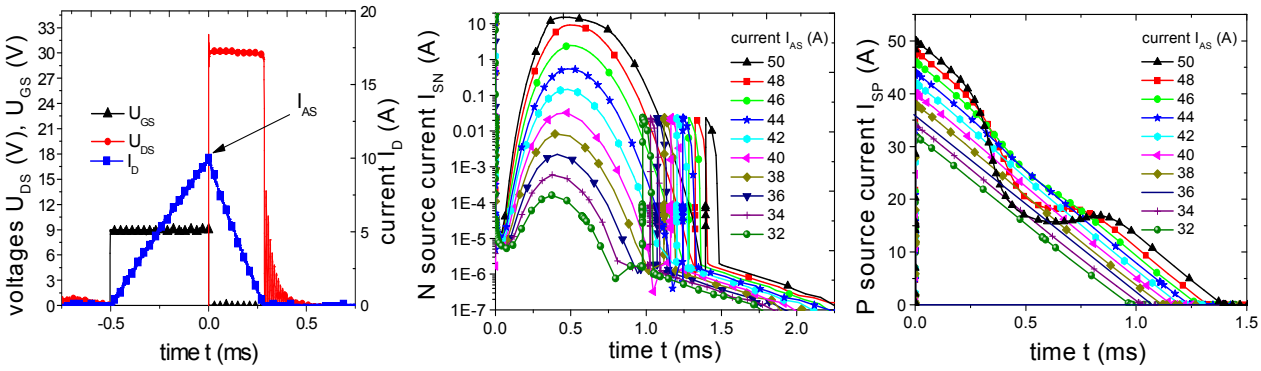
1. Introduction

The most serious failure mechanism of power MOSFET is a destructive damage during unclamped inductive switching (UIS) [1]. An unclamped inductive load represents an extremely stressful switching condition for the power MOSFET since all of the energy stored in the inductor during the on-state is dumped directly into the device during its turned off [2]. In this paper we present comparison between results obtained from the 2D and 3D electro-thermal simulations of the UIS test on power MOSFET. UIS test is commonly used to evaluate energy ruggedness (E_{AV}) of power MOSFETs. Using a 3D electro-thermal simulation allowed us to perfectly describe destructive breakdown mechanism of transistor during UIS test. Even though 3-D simulations provide better results, using them is more time consuming and need high computation capacity of workstation. For simulations a model of an n-channel vertical D-MOSFET was used. The geometry and doping profiles of structure cell corresponding to experimental DMOS transistors were defined by ISE TCAD 2D and 3D simulator. The considerable heat generation during the UIS test were simulated using thermodynamic model. In all simulations the drain contact connected to the ideal cooler with the ambient temperature T = 300 K was assumed as the bottom thermal boundary. The two most important parasitic elements in the structure are NPN bipolar transistor (BJT) and diode. From them particularly the parasitic bipolar transistor can have a detrimental effect on the D-MOSFET structure operation and reliability. Turning on of the parasitic BJT leads to second breakdown and therefore to the destruction of device. Due to the fact that simulator can not directly simulate destruction of device we assume opening of parasitic BJT as limiting state. To monitor opening of BJT source contact was split into two contacts – P and N source.

Normally during breakdown of transistor current flows through parasitic diode and therefore it flows through P source. Through N source flows only saturation current. After opening of the BJT, due to increased temperature, sizeable current start to flow through N source.

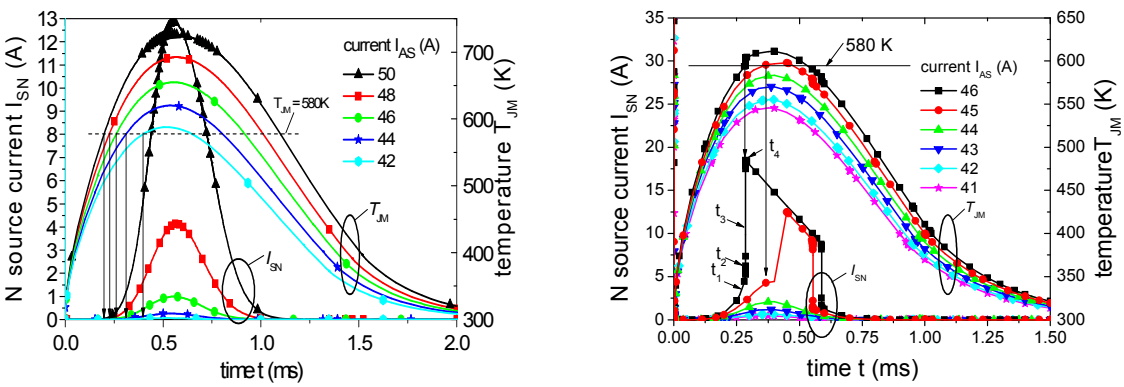
2. 2-D simulations of UIS



(a) *(b)* *(c)*

Fig.1: *a) Typical waveforms of voltages and current during UIS test. b,c) Current through N part (b) and P part (c) of source contact for I_{AS} = 32 – 50 A.*

On figure 1a typical waveforms of U_{DS}, U_{GS} and I_D during UIS test are displayed. On figures 1a and 1b are displayed currents through P and N part of emitor contact for different values of I_{AS} – maximal value of I_D during UIS test. One can see that with increasing I_{AS} maximal value of current through N source is increasing. Higher I_{AS} causes higher heating in volume of transistor. When temperature of blocking PN junction reaches T_J ~ 580K bipolar transistor is turned on, that is signalized by a rapid increase of the current through N source (Fig. 2a). But no generation of hot spots was observed using 2D simulation.



(a) *(b)*

Fig. 2: *Transients of temperature and current through N source for several I_{AS} currents obtained from 2-D (a) and 3-D simulations (b).*

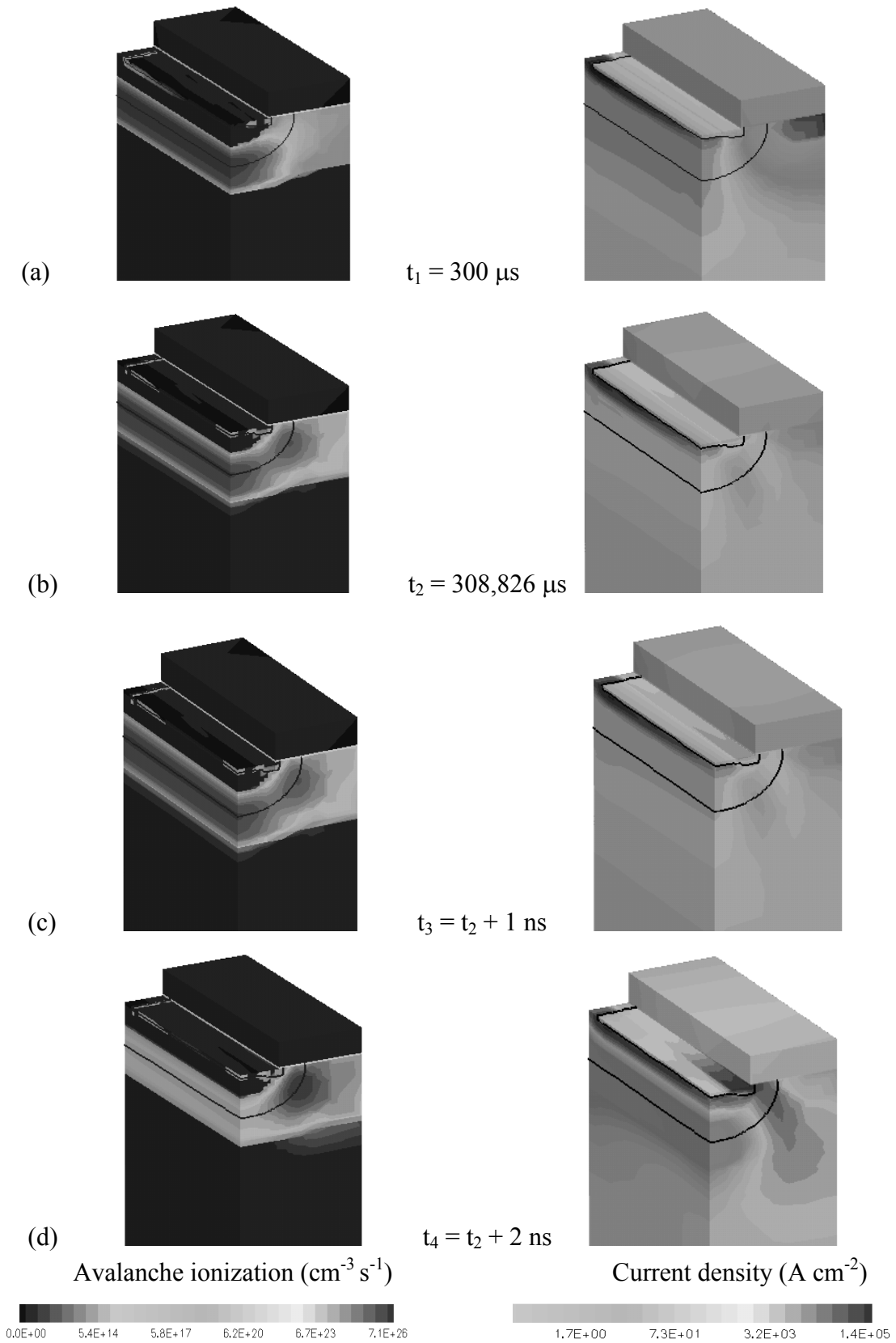


Fig. 3: *Creation of hot spot in 3-D model of power MOSFET during UIS test before and during turning on proces of parasitic BJT transistor for I_{AS} = 46 A*

3. 3-D simulations

In 2D simulations current through N source is rising with temperature smoothly. This indicates lack of hot spot effect. In a case of 3D simulations a hot spot generation was observed for tests with high I_{AS} where temperature in transistor volume reaches 580K and more. For lover temperatures no hot spots are generated and therefore such tests do not lead to destruction of device. Rapid increase with highly visible steep increase of current indicates opening of BJT. Creation of hot spot is depicted on fig.3. Times $t_1 - t_4$ correspond to times highlighted on figure 2b.

4. Conclusion

The results from 2-D and 3-D simulations of UIS are compared showing different waveforms of current I_{NS} through N source for higher I_{AS} currents. Hot spot generation in transistor volume which can be attributed to the experimental device failure was observed only in 3-D simulations. Although the 3-D simulations are much more time and memory consuming than the 2-D simulations, the 3-D simulations are needed to provide more correct physical interpretation of the experimental data of energetic ruggedness of power MOS transistors.

Acknowledgement

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