CALCULATION OF TUNNELING TRANSPORT TO ACOUSTIC EVALUATION OF INTERFACE STATE IN VERY THIN MOS STRUCTURES

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1. Introduction

The acoustoelectric effect in semiconductor structures has been shown to be an effective tool for the characterization of semiconductor interfaces. The acoustoelectric response signal (ARS) produced at the interface of the semiconductor structure when a longitudinal acoustic wave propagates through the structure [1] is sensitive to any changes in the space charge distribution in the interface region and its dependence on the external voltage ($U_{ac}^{0} - U_{g}$ curve) can be used to study of the density distribution of the interface states [2]. However, the leakage current represented by tunneling transport in the case of very thin oxide layers (< 10 nm) becomes a significant problem.

In the present contribution, the method of acoustic spectroscopy of interface states in MOS structures including the calculation of the tunneling transport is presented and verified by the results obtained on the representative MOS samples with very thin oxide layers prepared by NAOS (nitric acid oxidation) technology [3].

2. Theoretical principles

The ARS creation can be explained using the idea of an acoustic wave passing through the MOS structure characterized by the particular space charge region at the interface. The acoustic wave, following the pressure modulation of the charge at the MOS structure interface, evokes the change of the potential difference that manifests as an ARS. The ARS produced by a MOS structure can be then expressed, using the similarity with the case of electromechanical capacitance transducer [1] by the relation

$$U_{ac} = \phi_s \frac{p}{K_s} - \frac{Q_s(\phi_s)}{C_{ox}} \frac{p}{K_i} - \frac{Q_{it}(\phi_s)}{C_{ox}} \frac{p}{K_i}, \qquad (1)$$

where ϕ_s is the surface potential, Q_s is the semiconductor charge, Q_{it} is the trapped charge at the interface, C_{ox} is the oxide capacitance, K_s and K_i are the elastic moduli of the semiconductor and insulator, respectively and $p = p_0 \cos(\omega t\text{-}kx)$ is the acoustic pressure with the amplitude p_0. If the MOS structure without any interface states ($Q_{it} = 0$) is indexed as "ideal" the ARS amplitude in this case can be expressed as

$$U_{ac}^{0}ideal = \left| \frac{p_0}{K_s}\left(U_g - U_{fb}\right) + \frac{Q_s}{C_{ox}}\frac{K_i - K_s}{K_s K_i}\, p_0 \right|, \tag{2}$$

where the relation between the gate voltage and surface potential was used.

The tunneling current for SiO_2 layers with a thickness less than 10 nm, however influences the division of the applied voltage U_g between the semiconductor and the insulator layer and for the oxide layer thickness < 2 nm the whole applied voltage practically spreads across the semiconductor, especially in the range of inversion [4]. Concerning the tunneling process we take into account the transport of free charge curriers through the thin oxide layer caused by electric field where the tunneling current can be expressed in the form

$$J \sim a_1\left[\left(U_g - U_{fb}\right)^2 + a_2\right]\left[\exp\frac{a_3}{U_g - U_{fb}}\right], \tag{3}$$

where a_1, a_2, a_3 are the constants and the current is supposed to be thermally independent. The simulation of the "ideal" ARS amplitude inclusive the calculation of tunnel current contribution gives a new ARS $U_{ac}^{0}tunnel$. The interface charge can be then expressed using the new ideal and real ARS-voltage curves for MOS structure by the relation

$$Q_{it} = S\left|\left(U_{ac}^{0} - U_{ac}^{0}tunnel\right)\right|, \tag{4}$$

where $S = C_{ox} K_s / p_o$. The Eq. (4) allows then to determine the distribution of interface states from the measured and calculated ARS [2].

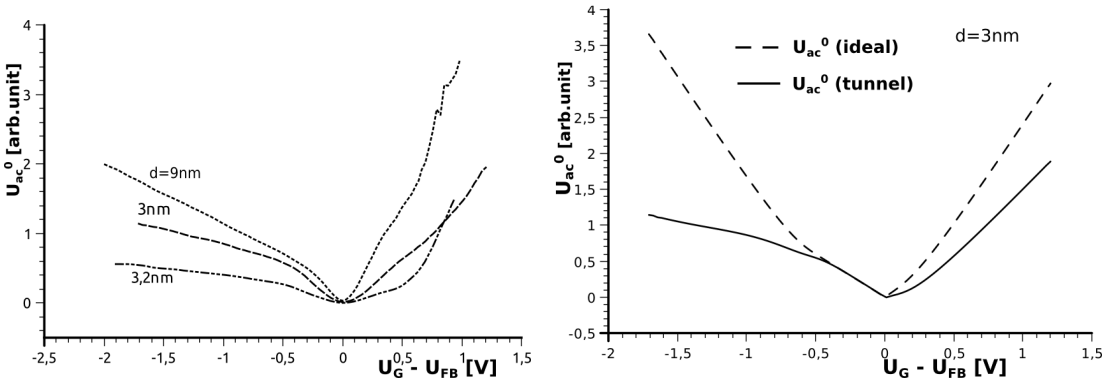
3. Experimental

The MOS structures were prepared on n-type Si substrates growing by NAOS technological procedure [3] fabricated on phosphorous doped n-type Si(100) wafer with ~ 10 Ωcm resistivity and had SiO_2 layers of thicknesses 3, 4 and 9 nm, respectively. The distribution of interface states was determined from the $U_{ac}^{0} - U_g$ characteristics using the theoretical principle described before. In order to lower the tunneling current flowing through the oxide layer another contact layer (silver paste) was deposited on Si-SiO_2 structures [5]. In

these cases the $U_{ac}^{0} - U_g$ curves contained the information about the interface states corresponding to the accumulation and originally obtained from Si-SiO_2-Al structure as well as the information about the interface states detected within depletion and inversion. The $U_{ac}^{0} - U_g$ measurements were performed using the equipment already described [2].

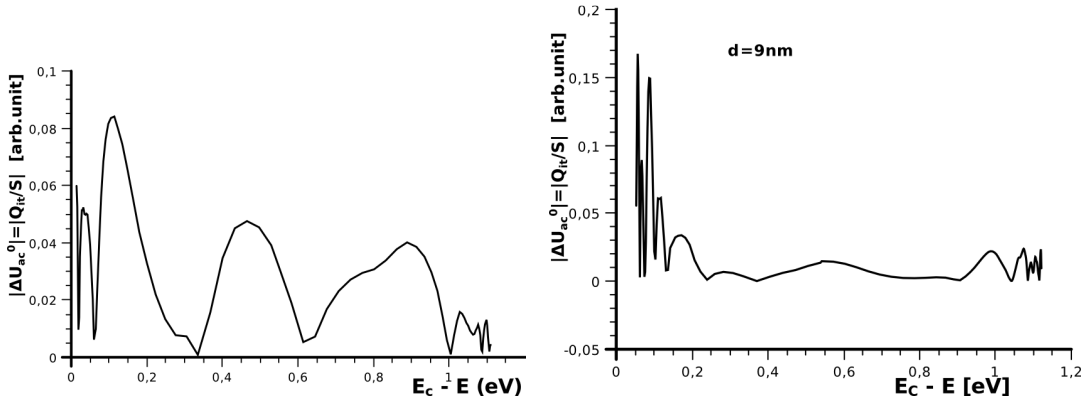
4. Results and discussion

Fig. 1 shows the measured curves of the ARS dependence on the gate bias voltage for the NAOS samples with tree different thicknesses (3, 3.2 and 9 nm) (a) and the theoretical calculation of the $U_{ac}^{0} - U_g$ curves both without and with tunnel transport calculation (b).



(a) *(b)*

Fig. 1: *The measured $U_{ac}^{0} - U_g$ curves for three samples (a) and calculated ideal curves showing the role of tunnel transport (b).*



(a) *(b)*

Fig. 2: *The distribution of interface states calculated from $U_{ac}^{0} - U_g$ curves for samples with oxide thickness 3 nm (a) and 9 nm (b).*

Fig. 2 shows the calculated distribution of interface states for two chosen NAOS samples. The obtained results coincide very well with the results obtained from the A-DLTS, the spectra of which presented the energy of interface states 0.40 eV (3 nm), 0.42 eV (3.2 nm) below the conduction band or are not detectable by A-DLTS (9 nm) [6]. The excellent agreements between the results obtained by different acoustic techniques definitely establish the acoustic spectroscopy as a useful tool for the interface states investigation.

4. Conclusion

The interface states distribution determined using $U_{ac}^{0} - U_{g}$ measurement including the tunnel transport allows us both to complete the acoustic investigation of MOS structures represented originally by the A-DLTS and also to provides information comparable with *C*-U_g and *G*-U_g measurements.

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