OTFT WITH PENTACENE-GATE DIELECTRIC INTERFACE MODIFIED BY SILICON NANOPARTICLES

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1. Introduction

Organic semiconducting thin films have been intensely studied due to their potential applications in organic electronics [1-4]. Pentacene, as one of the most investigated organic semiconductors, is regarded to be one of the leading candidates for the active semiconductor in organic thin film electronics. This is mainly due to its high intrinsic charge carrier mobility, the ambipolarity of the charge carrier transport, the excellent interface properties with different organic dielectrics, and the controllable growth of crystalline pentacene thin films. It is well known that the growth process and the quality of pentacene thin films are highly sensitive to the choice of the substrate material, the deposition rate, the substrate temperature, the film thickness, and the purity of the source material. The results show that the morphology, crystal structure and molecular ordering of the first organic monolayer(s) at the pentacene/dielectric interface are essential determinants of carrier transport phenomena [5]. It has been shown that carrier transport is mostly limited by space-charge effects [6]. Therefore, the charge accumulated on the semiconductor-gate insulator interface has great influence on device properties. Many theoretical studies have been carried out to clarify the device physics of Organic Thin Film Transistors (OTFT) [7, 8]. Their results call our attention to the control of the accumulated charge below the electrodes and in the channel region, which is crucial for carrier transport properties. One possibility to control the

accumulated charge is to use silicon nanoparticles (SiNPs) as was demonstrated by Weis [9]. These NPs serve as trapping centers and by design of their density it is possible to control the trapped charge, which has a strong impact on the carrier transport properties.

In this paper, we report on the properties of pentacene layers deposited on semi-conductor-gate insulator interfaces covered with SiNP monolayer prepared by the Langmuir-Blodgett (LB) method. We will also demonstrate the behaviour of a pentacene OTFT where the semiconductor-gate insulator interface is modified using SiNP monolayer. All characteristics are compared to a reference sample (without SiNPs) prepared in an otherwise identical way.

2. Experiment

For studying the growth of pentacene layers on SiNPs we used two different types of samples, A and B. The substrate treatment before SiNPs deposition (before pentacene growth) differs for both samples. In both cases heavily doped silicon wafers were used with a 40 nm thick thermally grown SiO_2 insulating layer. Prior to SiNPs deposition one substrate has the oxide surface cleaned for 10 min with UV light and ozone to obtain a hydrophilic surface (sample B), while the other substrate was treated in Hexamethyldisilazane (HMDS) vapour for 50 hours (sample A), resulting in different conditions for LB deposition. On both substrates the monolayer (ML) of SiNPs (Meliorum Technologies) stabilized with sodium n-dodecylbenzenesulfonic acid (DBSA) and with a size of 5 nm, was deposited by the LB method before pentacene evaporation (samples A-UV0, B-UV0). Because the nanoparticles are covered with DBSA film approximately 2.5 nm thick we have modified (thinned away) this SiNPs ML with UV light for different times (5, 10 and 15 minutes, samples A-UV5, A-UV10, A-UV15 and B-UV5, B-UV10, B-UV15 respectively). Pentacene films with a thickness of 40 nm were deposited on top of the SiNPs by thermal evaporation at a pressure of 10^{-3} Pa at 30 °C with a deposition rate of 0.030 nm/s, monitored by a quartz crystal microbalance. No further purification was performed for the commercially available pentacene material (Acros Organic). For device demonstration in the experiments we used top-contact pentacene OTFTs. For these devices after the deposition of pentacene, gold electrodes (source and drain) 40 nm thick were deposited on the semiconductor surface. The designed channel length (L) was 20 μm and 50 μm, respectively. The gate width (W) was 2.5 mm for all samples. For comparison, the reference sample C (OTFT without SiNPs) was prepared in an otherwise identical way.

Structural properties of the layers were characterized by micro-Raman spectroscopy (Jobin

Yvon HR800) at room temperature in backscattering geometry using He-Ne (633 nm) and Nd: YAG (532 nm) lasers. Standard AFM investigations were done using a Park System XE100 in non-contact mode with conductive Cr-Au cantilevers to study the surface morphology and the thickness of the pentacene layers. XRD measurements were carried out using a GE reflectometer (λ = 0.154 nm). Structural properties of the prepared layers were compared with the reference sample (sample C).

3. Results and discussion

The structure of pentacene layers is usually characterized by the presence of the thin-film and the bulk phase [10]. To analyze the structure, micro-Raman spectroscopy was employed [11, 12]. The evaluation of the ratio (α) of the integral peak intensities at 1154 and 1158 cm^{-1} ($\alpha = Int_{1154} / Int_{1158}$) provides information on the thin film and bulk phase across the scanned area of the pentacene layer. If this ratio is close to 1, the structure is normally suitable for the preparation of OTFTs with high carrier mobility. A ratio of about 0.5 reflects a low fraction of the thin-film phase in the pentacene layer, hence usually low channel mobility in OTFTs. The Raman measurements of our samples where the semiconductor-gate dielectric interface was modified with SiNPs show that the average value of α is between 0.8 and 1.0.

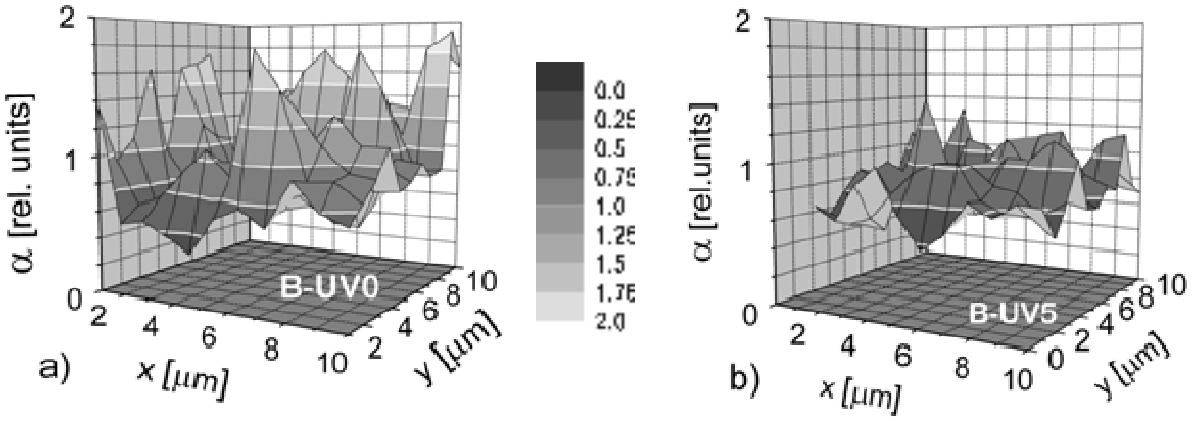

Fig. 1. *Raman spectra intensity ratio mapping of 40 nm thick pentacene layer grown on hydrophilic semiconductor-gate insulator (SiO_2) surface covered with SiNPs monolayer a) as deposited b) with UV and ozone pre-treatment for 5 minutes.*

We have tested if UV ozone treatment changes α. Fig 1 shows maps of α on a 10×10 mm^2 area for 40 nm pentacene layer grown on the hydrophilic surface of SiO_2 gate insulator layer covered with a SiNPs monolayer. α depends on the SiNP treatment before pentacene

deposition as is visible from Fig 1. Using 5 min UV ozone treatment we have obtained pentacene layers with slightly lower α but better structural homogeneity. X-ray scattering data (not shown) confirm that the films are well ordered, with well-defined Bragg reflections and narrow rocking widths (0.1 degrees and below), as well as pronounced Kiessig interferences [3, 4]. The AFM analysis of the pentacene layers reveals that the different surface treatment of SiO_2 gate insulators (hydrophobic or hydrophilic) before SiNPs monolayer deposition has a distinct influence on the surface morphology.

Fig. 2 shows the dependence of the saturation current and output characteristics (for $U_G = -20$ V) as a function of storage time of the top contact OTFT where the pentacene layer was grown on a semiconductor-gate dielectric interface modified with SiNPs (sample A) and without SiNPs (sample C). The samples were measured after storage under ambient conditions for 54 and 85 days, respectively. The saturation current for sample C measured after processing shows a ~ 2 times higher saturation current in comparison with sample A after UV treatment (Fig 2a). Interestingly, the saturation current of OTFTs with SiNPs is increasing (~ 2.5 ×) with storage time (85 days) in comparison to OTFTs without SiNPs, which decrease similarly after 54 days (Fig. 2b).

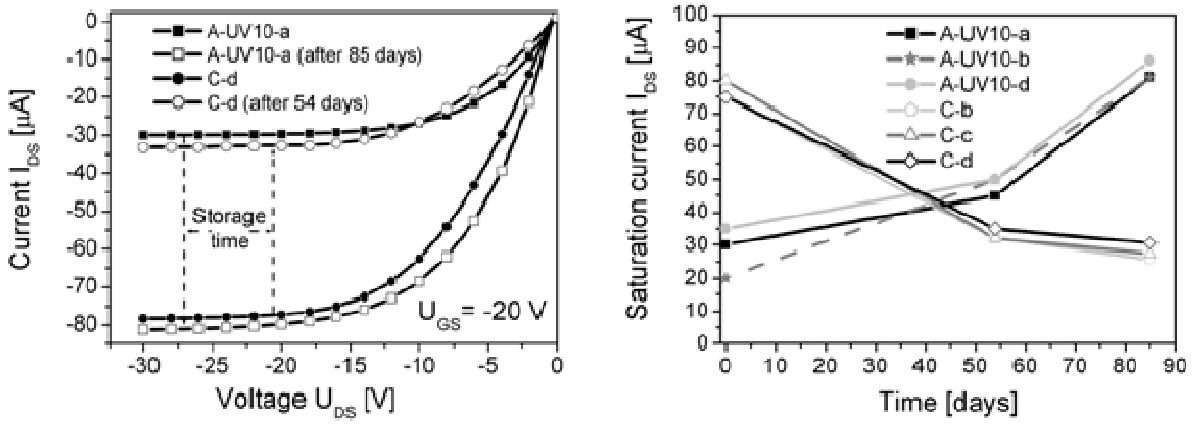

Fig. 2. *Time dependence comparison of top-contact pentacene OTFT with DBSA-stabilized SiNPs (sample A-UV10) and without SiNPs (sample C) respectively a) output characteristics b) saturation current characteristics.*

The reason of higher time stability and increasing of saturation current behaviour of pentacene OTFT after storage time where the semiconductor-gate insulator interface is modified using SiNP monolayer may be interpreted by the different structural quality and

possibly the presence of charged defects at the interface. The detailed analysis is presently underway.

4. Conclusion

We have for the first time investigated the structural and electrical properties of pentacene OTFT deposited on the semiconductor-gate insulator interface covered with SiNPs monolayer prepared by the LB method and compared these to a reference sample (without SiNPs). The micro-Raman, AFM and XRD measurements confirmed that the pentacene layer deposited on the semiconductor-gate insulator interface covered with a SiNPs monolayer on both hydrophobic and hydrophilic surfaces changes the structure. The Raman measurements show that the average value of α is between 0.8 and 1.0. The different structural quality of pentacene leads to better OTFTs electrical characteristics mainly saturation current of OTFTs with SiNPs increasing ($\sim 2.5 \times$) with storing time (85 days) in comparison to OTFTs without SiNPs, which decrease similarly after 85 days.

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