OFF-STATE STRESS AND PULSE RESPONSE INVESTIGATION OF InAlN/GaN HFET

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1. Introduction

The GaN-based heterostructure is a promising candidate as a field-effect transistor (HFET) device due to its wide band gap, superior carrier saturation velocity, thermal conductivity, and high breakdown field all of which are required for high temperature and high speed application. Most research on HFETs has focused on understanding and improving the performance, structure and fabrication processes. Because of lack of sizable GaN substrates , GaN based materials are grown on foreign substrates, e.g. Si, SiC or sapphire. Lattice constants of AlN and 6H-SiC suggest a lattice mismatch of 1.2 % of the AlN layer but nowadays such SiC substrates are relatively high-priced. On the other hand a Si is a promising substrate for GaN growth because of its high electrical and thermal conductivity, larger wafer size at low cost but there is problematic is the lattice mismatch of 17% to GaN. Moreover, Si has an advantage that integrated circuits can be formed using monolithic integration, that means combining by GaN-based high-power and high-speed devices with Si integrated circuits [1].

Several requirements exist for a buffer structure suitable for such devices. Epitaxial GaN layers were successfully grown on Si substrate with AlN [2], or AlGaN [3] buffer layer. The large difference in thermal expansion coefficient between GaN and Si generates residual tensile stress in GaN and many cracks in the grown layers [3]. Therefore the residual tensile stress is the most serious problem for the growth of GaN on Si [4]. However, achieving acceptable reliability and stability under continuous high performance operations is still needed for the commercialization of microwave devices and monolithic integrated circuits.

In this study $In_{0.18}Al_{0.82}N$/GaN HFETs were off-state tested under high drain bias, I-V characteristics were measured using standard DC voltage source (drain-source, gate-source). Subsequently drain current responses on pulse gate-source voltage for various drain-source voltages were recorded and analysed.

2. Experimental

Investigated InAlN/GaN samples were grown on semi-insulating Si (111) substrates by metal-organic vapour phase epitaxy (Fig. 1).

Conventional processing steps were used for InAlN/GaN HFET preparation. For ohmic contact formation the metallization layer stack of Ti/Al/Ni/Au (12/200/40/100 nm) annealed for 40 s at 850°C (AT) was used. The gate contact with the gate length of 2 μm and width of 200 μm was formed using Ni/Au (10/300 nm) metallization.

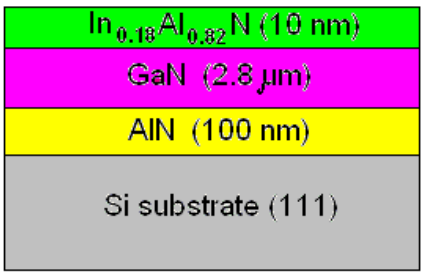

Fig. 1: *Vertical structure of investigated sample.*

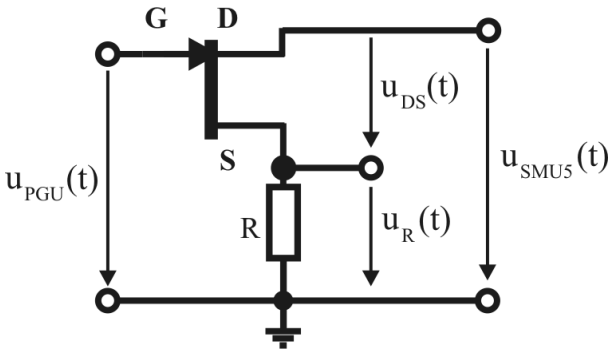

Fig. 2: *Electrical circuit of pulse measurements.*

Static and pulse I-V characteristics of the fabricated HFETs were measured using Agilent 4155C parameter analyzer, Agilent DSO 5054A oscilloscope with wolfram contact probes connected to the expanded contacts. Static output and transfer I-V characteristics were measured using analyser's built-in voltage and current meters. For pulse measurements investigated HFET was connected to the electrical circuit (Fig. 2), gate-source voltage $u_{PGU}(t)$ is connected to the pulse source with frequency 1 kHz and pulse width 10 μs changing in the range (– 5 V, + 1 V). Drain-source voltage $u_{SMU5}(t)$ is rising in 0.5 V steps each 0.5 s in the range (+ 0V, + 10 V) as shown in Fig.3. Drain current $i_R(t) = u_R(t)/R$ corresponds to an average value calculated during the pulse after transient response.

The resistivity R = 10 Ω was chosen as low as possible considering a sufficient oscilloscope resolution. Particular pulse output I-V characteristic is processed as a drain current $i_R(t)$ versus stepping drain-source voltage $u_{SMU5}(t)$ from the time response of investigated HFET.

The off-state stress conditions for the measurements can be described as follows:

a) first the virgin devices were characterised in details before the stress,
b) off-state gate-source voltage – 4.4 V was nearby the pinch-off voltage, drain-source voltage ~ 30 V was below the breakdown voltage, which varies for each sample and during the stress in duration of 60 min the gate and drain currents were measured continuously,
c) stress measurement was interrupted after 10 min and detailed characterisation of device was performed, the stressed devices were characterized after total stress time of 60 min,
d) after the stress the devices were left for 30 min without bias connection and were characterised in details in order to evaluate the stress-recovery conditions.

3. Results and discussion

The static output I-V characteristic of $In_{0.18}Al_{0.82}N$/GaN HFET (Fig. 4) show that in the linear region the HFET acts like a resistor with impedance controlled by gate voltage. In the saturation region the maximum drain current $I_{ds} \approx 0.44$ A/mm for $V_{ds} = 6$ V was reached. For $V_{gs} > -1$ V there are many free carriers in the HFET channel resulting in a velocity and drain-source current decrease. The device has pinch-off at $V_{gs} \approx -4.4$ V.

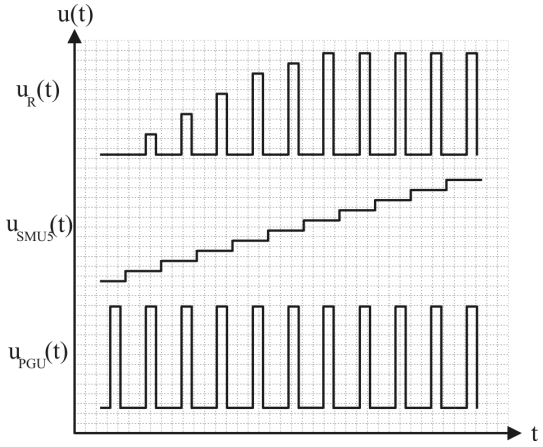

Fig. 3: *Pulse response of investigated HFET.*

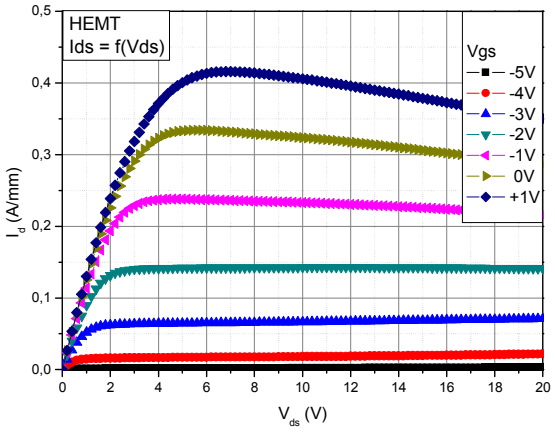

Fig. 4: *Static output I-V characteristics.*

The drain and gate currents of the InAlN/GaN HFET were measured continuously during the off-state stress (V_{DS} = 30 V, V_G = – 4.4 V), as shown in Fig. 5a.b. The drain/gate current decreased continuously with the stress time and in similar behaviour. The stress was interrupted after 10 min to perform detailed characterisation of the devices. A partial increase of the drain/gate current was observed after this interruption, which indicates on some recovery effect. During the next stress, i.e. between 10 and 60 min of the total stress time, the drain/gate current follows the previous stress vs time dependences. The devices were characterized in details after the total stress time of 60 min, as well as after 30 min without the stress, the output I-V characteristics show permanent off-state stress degradation as shown in Fig.6.

(a) (b)

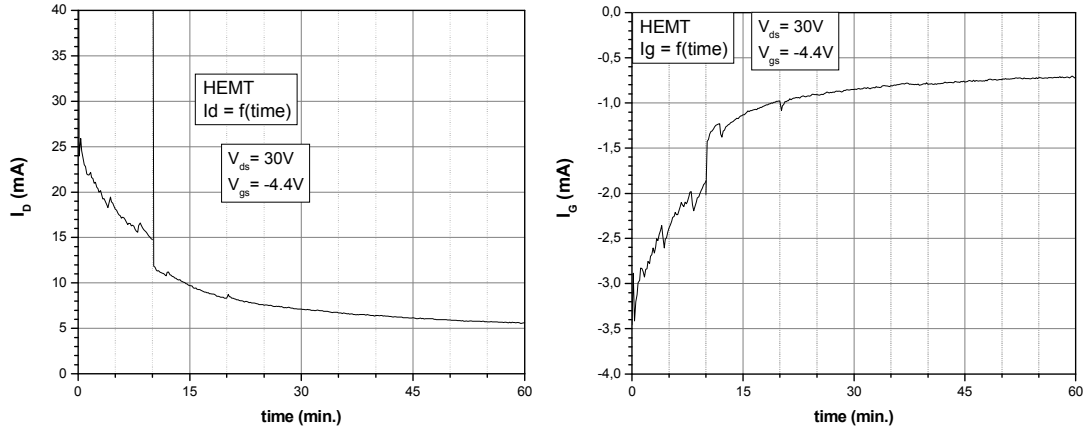

Fig 5: *Time dependence of* (a) *drain current and* (b) *gate current during off-state stress.*

(a) (b)

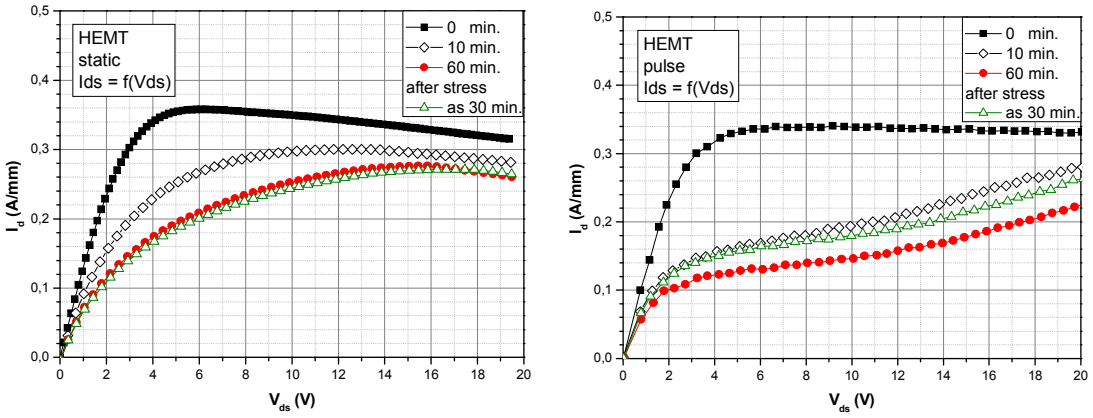

Fig. 6: *Static* (a) *and pulse* (b) *output I–V characteristics of investigated HFET.*

In comparison of static and pulse measurements the reduction of temperature current collapse is reduced before off-state stress measurements (Fig.6a,b). During the off-state stress the traps in the HFET structure are activated and give rise to trap assisted current collapse. This effect gives rise to the considerable reduction of I_d after 10 still after 60 min. In the pulse measurements the effect is more expressive (Fig 6b). The recovery after 30 min in static measurements is negligible but rise in the case of pulse measurements.

4. Conclusions

Static performance of InAlN/GaN HFETs with AlN buffer layer prepared at different conditions were analysed before, during and after the off-state stress. The static output I-V characteristics show the maximum drain current $I_d \approx 0{,}44$ A/mm for $V_{gs} = 6$ V, the device has pinch-off at $V_{gs} \approx -4.4$ V. The drain and gate currents of the InAlN/GaN HFET were measured continuously during the off-state stress ($V_{ds} = 30$ V, $V_{gs} = -4.4$ V), a partial increase of the drain/gate current was observed after this interruption, which indicates on some recovery effect. The devices were characterised in details after the total stress time of 60 min., as well as after 30 min without the stress, the output I-V characteristic show permanent off-state stress degradation. This effect will be studied in details in the next.

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